# A Radial Exploration Approach to Manufacturing Yield Estimation and Design Centering

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Abstract-An integrated approach to manufacturing yield estimation and design centering is presented in which linear searches along "radial" directions within the multiparameter component space are used to locate points on the boundary of the feasible region for a given nominal design and a set of component tolerances. This set of boundary points enables the volume of the feasible region, and hence the manufacturing yield, to be estimated by using a newly developed computational technique. For linear frequency-domain circuit behavior, application of the tracking-sensitivity algorithm further enhances the searching efficiency. The boundary points are also used within a practical design centering algorithm which minimizes the asymmetry of the feasible region around the nominal design. Iterative application of this process leads to a better centered design. Examples of the application of this algorithm to circuit design are given. The results indicate that the radial exploration approach to yield estimation and design centering is effective in practice, computationally cheap, and applicable to many situations in practical circuit design.

#### I. INTRODUCTION

**P**RACTICAL circuits have to be designed in the face of uncertainties. These may be the statistical variations in component values due to manufacturing tolerances, or environmental factors such as temperature or humidity. The effect of the ensuing variations in component values is that the circuit's response will also exhibit variation from one sample to another. In this case the manufacturing yield-which is the proportion of manufactured circuits which meet the performance specifications-is of considerable interest to the designer. Monte Carlo methods may be used to simulate component variation in order to esimate the yield, but can be rather expensive in terms of computing time. In any case, such simulations only enable the designer to estimate the yield of a given design. The general problem of obtaining a better design (e.g., with a higher yield) still remains essentially unanswered.

Although a considerable amount of research is now in progress [1]–[12], the solutions presented so far are by no means general or demonstrably the most appropriate to practical circuit design. Most of the effort has been concentrated on the first half of the problem, by developing more efficient alternatives to Monte Carlo methods for yield estimation [10]–[17]. For the second half of the

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problem—that of *increasing* the yield—the solution can involve a change in nominal component values with the tolerances held fixed (design centering), or vice versa (tolerance assignment), or a combination of the two approaches. Design centering is important in that it involves no change in component cost and, even if tolerance assignment is attempted, will usually be carried out first.

This paper proposes a new radial exploration approach to yield estimation and design centering, an approach in which the information obtained during the yield estimation stage is used, at little additional cost, to improve the existing design. The potential savings of the approach have been demonstrated using test circuits containing up to 58 variable components.

## II. MANUFACTURING YIELD

Consider a circuit in which there are *m* variable components  $p_1, p_2, \dots, p_m$  such that the *i*th component  $p_i$  varies between its upper limit  $\overline{p_i}$  and lower limit  $p_i$  with a probability density function (PDF)  $\phi_i(p_i)$ .<sup>1</sup> Let  $\overline{q_j}$  and  $q_j$  be the upper and lower specification limits on the *j*th of the circuit's *n* responses of interest. The manufacturing yield can then be expressed as

$$Y = \int_{\underline{p}_m}^{\overline{p}_m} \cdots \int_{\underline{p}_1}^{\overline{p}_1} g(p_1, \cdots, p_m) \phi(p_1, \cdots, p_m) dp_1 \cdots dp_m$$
(1)

where  $\phi(p_1, \dots, p_m)$  is the joint *pdf* of the *m* variable components, and  $g(p_1, \dots, p_m)$  is a testing function which indicates acceptance or rejection of the circuit under consideration, viz:

$$g(p_1, \cdots, p_m) = 1, \quad \text{if } q_j \leq q_j(p) \leq \bar{q}_j; \ j = 1, \cdots, n$$
$$= 0, \quad \text{otherwise.} \qquad (2)$$

Alternatively, the yield can be expressed as a mathematical expectation of  $g(p_1, \dots, p_m)$  with respect to the *pdf*  $\phi(p_1, \dots, p_m)$ :

$$Y = \langle g(p_1, \cdots, p_m) \rangle \qquad \text{w.r.t. } \phi(p_1, \cdots, p_m). \tag{3}$$

16: For nonlinear circuits, a search involving a small number of circuit analyses may be involved. For linear circuits, a very efficient procedure [17], [18] is available.

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In practice, an estimate  $\hat{Y}$  of this expectation can be obtained by simulating a number (N) of the circuits according to the *pdf*  $\phi(p_1, \dots, p_m)$  and then applying the testing function (2), such that

$$\hat{Y} = \frac{1}{N} \sum_{i=1}^{N} g(p_1, \cdots, p_m).$$
 (4)

The estimate  $\hat{Y}$  can also be interpreted as the proportion of circuits which pass the specification test, and is the most commonly understood meaning of the definition of manufacturing yield.

## III. RADIAL EXPLORATION

For notational convenience it is useful to define the various regions of interest in the component space. Let the tolerance region be denoted by T, where

$$T \stackrel{\triangle}{=} \left\{ p | p_i \leq p_i \leq \bar{p}_i; i = 1, 2, \cdots, m \right\}$$
(5a)

and the acceptance region by A, where

$$A \triangleq \left\{ p | \underline{q}_j \leqslant q_j(p) \leqslant \overline{q}_j; j = 1, 2, \cdots, n \right\}.$$
 (5b)

The feasible region F is then the intersection of the tolerance and acceptance regions:

$$F = A \cap T. \tag{6}$$

Using these definitions, the manufacturing yield Y as given by (1) can now be expressed as

$$Y = \int \cdots_{F} \int \phi(p_1, \cdots, p_m) dp_1 \cdots dp_m.$$
(7)

The manufacturing yield can also be expressed in terms of the "weighted" volumes of the tolerance and feasible regions. For the simple case of uniform and uncorrelated component distributions, the yield is simply the ratio of the feasible  $(V_F)$  and tolerance  $(V_T)$  volumes:

$$Y = \frac{V_F}{V_T}.$$
 (8)

On the basis of extensive experimental evidence it is suggested that an assessment of Y can be made (which may not necessarily be an unbiased estimator of Y, but is nevertheless useful for controlling the yield improvement) in the following way. First, in multiparameter component space, a number of lines having random directions are generated, in each case passing through the nominal design. For each such line, and in both directions away from the nominal design, the distances  $r_F$  and  $r_T$  to the edges of the feasible and tolerance regions are determined (Fig. 1). Again in both directions, the normalized distance  $r_0(=r_F/r_T)$  to the feasible region boundary is calculated so that two distances,  $r_0^+$  and  $r_0^-$ , are associated with each line. The proposed assessment of Y is then

$$\hat{Y} = \frac{1}{2L} \sum_{j=1}^{L} \left( r_{0_j}^+ \right)^m + \left( r_{0_j}^- \right)^m \tag{9}$$

where L is the number of randomly generated lines, and



Fig. 1. Illustrating the distances  $r_F$  and  $r_T$  to the boundaries of the feasible and tolerance regions, respectively, from the nominal design. Two examples are shown.



Fig. 2. For circular and concentric volumes  $V_F$  and  $V_T$  in two dimensions, the ratio of the two volumes is equal to  $(r_F/r_T)^2$ .

 $r_{0_j}^+$  and  $r_{0_j}^-$  are the normalized distances associated with the *j*th line.

A single contribution (e.g.,  $(r_{0_j})^m$  for a specific *j*) to the summation in (9) may be viewed as the result of a onesample experiment to estimate the ratio of two volumes. For example, for two variable components, and for the special case of circular and concentric volumes  $V_F$  and  $V_T$ (Fig. 2), the ratio of volumes is  $(r_F/r_T)^2$ ; for *m*-dimensional spherical volumes the ratio would be  $(r_F/r_T)^m$ . A succession of such (independent) samples of relative volume is then used, in (9), to provide a better estimate, just as a Monte Carlo analysis employs a series of onesample experiments of circuit success or failure.

Although the derivation of (9) has not been mathematically rigorous, the algorithm (see Appendix A) for yield estimation based on this expression has been subjected to extensive testing both with circuits ranging in size from 7 to 58 variable components as well as with two- and three-dimensional geometric patterns for which the yield is known. In all cases very satisfactory confirmation was obtained. For the circuits, Table I compares yield estimates with those obtained from a 500-sample Monte Carlo analysis. For the geometric patterns, Table II allows estimated relative volumes to be compared with known exact values.

TABLE I Comparison of Yield Estimates Obtained by the Radial Exploration and Monte Carlo Methods for Various Designs of Three Different Circuits; the Relative Costs are also Indicated

Circuit	Yie	Cost of			
Circuit	Radial Exploration		Monte Carlo		Radial Exploration
	Number of lines			95 % Confidence Limits	Relative to 500 sample Monte Carlo
Directional filter (Fig 6)	20 50 100 200 500	54.5 53.8 58.6 57.8 56.2	52.4 " "	47.9-56.9	0.07 0.14 0.25 0.47 1.13
Active high-pass filter (Fig 9)	50 50 100 100	63.6 84.5 62.9 86.4	61.4 89.8 61.4 89.2	57.0-65.8 87.1-92.5 57.0-65.8 86.4-92.0	0.17 0.12 0.34 0.25
Band-pass filter (Fig 4)	50 50 50 50	44.0 92.7 61.1 99.8	39.8 91.4 61.0 99.6	35.4-44.2 88.8-94.0 56.6-65.4 99.0-100.0	0.18 0.14 0.13 0.11



FIGURE	EXACT RATIO	RADIAL APPROXIMATION
+ 2- dimensional	0, 785	0.800
2-dimensional	0.385	0.382
+) 2-dimensional	0.393	0,400
2-dimensional	0.375	0, 345
+ 3-dimensional	0, 524	0.555

### IV. DESIGN CENTERING ALGORITHM

In general, the manufacturing yield is less than the maximum attainable because the tolerance region is not centered within the region of acceptability. However, because the yield estimation algorithm described earlier provides information concerning the *feasible* region, we em-



Fig. 3. Definition of the asymmetry vector and asymmetry level for a line in multidimensional component space. Asymmetry level for line shown =  $|r_0^+ - r_0^-|$ .

ploy the asymmetry of the feasible region relative to the current tolerance region as the basis of a new design centering procedure.

A measure of asymmetry—the asymmetry vector—is assigned to each of the lines generated in the yield estimation algorithm, and is the difference between its two feasible lengths  $r_0^+$  and  $r_0^-$  (Fig. 3). Thus the asymmetry associated with a line has both magnitude and direction. The *direction* of movement of the design centre (i.e., the nominal component values) is taken to be that of the vector sum of the individual (line) asymmetry vectors. The magnitude of movement is chosen somewhat empirically. A choice that has been found suitable in practice is obtained by dividing the magnitude of the vector sum of the asymmetry vectors by the number of "important lines." Initially, a line is regarded as important if its asymmetry level (which is the difference between its two feasible lengths (Fig. 3)) exceeds a given value (e.g., 0.9), but the critical level is gradually reduced as design centering proceeds. The centering scheme terminates either when each of the asymmetry levels has fallen below a minimum value (which, in the examples reported here, is 0.1), or after undergoing a specified number of design centering iterations. The algorithm is described in some detail in Appendix B.

## V. EXPERIMENTAL RESULTS

The algorithms for yield estimation and design centering have been implemented in Fortran on a CDC 6500 computer. The program can handle the frequency-domain behavior of linear circuits containing the basic two-terminal passive components as well as independent sources and mutual conductances. Simple linear models of transistors and operational amplifiers have been incorporated.

The program was first applied to the bandpass filter shown in Fig. 4, for which the performance specifications are listed in Table III. The eight parameters so indicated in Fig. 4 were assumed to be subject to variation within specified tolerances. The results associated with two different component tolerances are shown in Fig. 5; in each case, 50 lines at each of five frequencies were used at each



Fig. 4. Bandpass filter. Component values in ohms, picofarads and millihenries.

TABLE III Performance Specifications for the Bandpass Filter of Fig. 4

	Loss specification			
Frequency range	Minimum	Maximum		
<240 Hz	L <sub>0</sub> +36.5 dB	-		
360 Hz to 490 Hz	L <sub>O</sub> -0.5 dB	L <sub>o</sub> +2.1 dB		
>700 Hz	L <sub>0</sub> +36.5 dB	-		
	L <sub>o</sub> = 8.86 dB			

iteration of the design centering procedure. For the 5 percent component tolerances (Fig. 5(a)) the design is seen to converge from an initial yield estimate of 44 percent to a final estimate of 91 percent. The corresponding 500-sample Monte Carlo estimates are also shown. The CPU-times associated with each iteration are shown in rectangles, and those associated with the 500-sample Monte Carlo estimates in triangles. Fig. 5(b) shows the results obtained for 2-percent component tolerances, but with the same initial design. In general, it is seen that the cost of a complete design centering exercise can be considerably less than that of a 500-sample Monte Carlo analysis of just the initial design.

The program was also used to improve the design of an active filter employing two operational amplifiers, as well as the design of a 58-component filter containing resistances, capacitances, and inductances. As well as to obtain additional experimental evidence in support of the proposed algorithms, the main objective was to test the hypothesis that, since the radial exploration approach is based on a statistical sampling of component space, its computational cost in terms of the number of circuit analyses is largely independent of dimensionality. Fig. 6 shows the form of the filter circuit and Fig. 7 shows the specifications on passband loss and return loss. Fig. 8 shows the results of the application of the design centering procedure for the case when 100 lines were used; for the initial design the result and cost of a 500-sample Monte Carlo analysis is also shown.





Fig. 6. A directional filter. CC'-AA' is the low-band (LB) section CC'-BB' is the high-band (HB) section.

Fig. 9 shows the circuit of the active filter and its gain specifications. All the resistors in this circuit were assigned tolerances of 0.1 percent, and the two capacitors were assigned tolerances of 0.5 percent. Fig. 10 shows the yield trajectories for the cases in which 50 and 100 lines were used. Again, the computational costs are identified.



Fig. 7. Passband and return loss specifications for the directional filter of Fig. 6.

(b)



Fig. 8. Yield trajectory and CPU times relating to the directional filter example of Fig. 6.

The effect of differing number of radial lines is indicated within Table I for the 58-variable component circuit of Fig. 6. As the number of lines increased from 20 to 500 the yield estimates exhibited little variation and were comparable with the results of a 500-sample Monte Carlo analysis.

Elsewhere [19] we have reported the successful extension of the yield estimation and design centering procedure to the cases in which the component distributions are not uniform, as well as the approach that can be adopted when certain LC pairs in the filter of Fig. 6 are tuned manually to within a given accuracy before assembly.



Fig. 9. An active high-pass filter and its gain specifications. (a) Circuit diagram. (b) Equivalent circuit of the operational amplifier. (c) Gain specification.

$C_2 = C_5 = 15 \text{ nF}, R_2 = R_3 = 2 \text{ k}\Omega$	$R_{in} = 1 \ \mathrm{M}\Omega$
$R_1 = 1.861 \text{ k}\Omega, R_4 = 60.479 \text{ k}\Omega$	$q = 10^8$
$R_5 = 318 \text{ k}\Omega$	om to
$R_1 - R_5$ have 0.1 -percent tolerances	$R_e = 10^3$
$C_1, C_2$ have 0.5 -percent tolerances.	$C_e = 15.915$ F.

#### VI. CONCLUSIONS AND EXTENSIONS

A design-centering scheme based on the radial exploration of multiparameter component space has been described, and its application to circuits of various sizes has shown it to be effective and computationally attractive. In general, the cost of a complete design-centering exercise is considerably less than that of a 500-sample Monte Carlo analysis of the initial design. Although tested exclusively with linear circuits, the scheme is equally applicable to dc and time-domain design, as well as to the design of other physical systems. The results of its application to circuits containing from 7 to 58 variable components tend to support the hypothesis that the number of circuit analyses required is relatively independent of the number of variable parameters in the circuit.

As explained earlier, the basis of the yield estimation algorithm is essentially intuitive. A rigorous mathematical derivation of the algorithm would not only be useful in its own right, but might also provide a relation between the accuracy of the yield estimate and the number of lines.



Fig. 10. Yield trajectories and CPU times relating to the active filter example of Fig. 9. (a) Radial method using 50 directions. (b) Radial method using 100 directions. ⊽ 500-sample Monte Carlo estimate.

The scheme appears capable of yielding additional information of value to the designer. For example, some form of projection of the points on the feasible region boundary onto the component directions can provide an indicator of yield sensitivity, and may be a suitable means whereby the radial exploration approach can be extended to include tolerance assignment. It is also possible that the information obtained during radial exploration can be used by the designer to examine the tradeoff between specifications and yield; since specifications, normally considered to be fixed, are often open to negotiation.

## Appendix A

## THE RADIAL EXPLORATION ALGORITHM FOR YIELD ESTIMATION

1) Compute the impedance matrix at the first frequency. (In practice, LU factors will suffice.)

2) Generate a line in a random direction and find its intersections with the tolerance region.

3) Search in both directions from the nominal design to locate its intersection with the feasible region.

4) Compute the normalized distances  $r_{0j}^+$  and  $r_{0j}^-$ .

5) Repeat steps 2 to 4 for each of L lines.

6) Repeat steps 1 to 5 for each of the F frequencies, using the same set of L random directions as for the first frequency, and retain the minimum value of  $r_0^+$  and  $r_0^-$  for each line.

7) Use (9) to compute the estimate of yield.

#### APPENDIX B

## THE RADIAL EXPLORATION ALGORITHM FOR YIELD ESTIMATION AND DESIGN CENTERING

1) Set the iteration counter I to 1 and apply the yield estimation algorithm described in Appendix A, using I to initiate the random number generator used in that algorithm.

2) Find the SUM of the individual asymmetry vectors (Fig. 3).

3) Set the critical asymmetry level to its initial value (=0.9).

4) Count the number of important lines *IL* at this asymmetry level.

5) If IL=0, reduce the critical asymmetry level by 0.2 and repeat step 4.

6) If *IL* is still equal to zero when the critical asymmetry level has been reduced below a specified level (e.g., 0.1), no more improvement can occur, so STOP.

7) If  $IL \neq 0$ , find the new design by updating the existing design by the displacement vector SUM/IL.

8) Increasing I by one and apply the yield estimation algorithm (Appendix A).

9) If the new design is found to be inferior in terms of yield, or is nonfeasible, discard it. Increase I by one to move into a different block of random numbers and reapply the yield estimation algorithm followed by steps 2 to 7.

10) If the new design is better in terms of yield, accept this design and increase I by one. Apply the yield estimation algorithm and repeat steps 2 to 9 until an optimum design results from step 6, or I exceeds the maximum specified number of iterations.

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#### References

- B. J. Karafin, "The optimum assignment of component tolerances [1]
- J. Katalini, The optimum assignment of component [2]
- [3] ming approach to optimal design centering, tolerancing and tuning," IEEE Trans. Circuits Syst., vol. CAS-23, pp. 155-165, Mar. 1976.
- N. J. Elias "New statistical methods for assigning device toler-[4] G. Kjellstrom and L. Taxen, "On the efficient use of stochastic
- [5] optimization in network design," IEEE, ISCAS 76, pp. 714-717. P. W. Becker and F. Jensen, Design of Systems and Circuits for
- [6] Maximum Reliability or Maximum Production Yield. New York: McGraw-Hill, 1977.
- . M. Butler, E. Cohen, N. J. Elias, J. J. Golembeski and R. G. [7] Е Olsen, "CAPITOL--Circuit analysis program including toleranc-IEEE, ISCAS 77, pp. 570-574. ing
- B. J. Karafin, "The general component tolerance assignment prob-lem in electrical networks," Ph.D. thesis, Univ. of Pennsylvania, [8] 1974.
- S. W. Director and G. D. Hachtel, "The simplicial approximation [9] approach to design centering," IEEE Trans. Circuit Syst., vol. CAS-24, pp. 363-372, July 1977.
- J. W. Bandler and H. L. Abdel-Malek, "Optimal centering, toler-[10] ancing and yield determination using multidimensional approxi-mations," *IEEE, ISCAS* 77, pp. 219–222. —, "Yield estimation for efficient design centering assuming arbitrary statistical distributions," in *Proc. IEEE,* CADEMICS,
- [11]
- [11] —, "Yield estimation for efficient design centering assuming arbitrary statistical distributions," in *Proc. IEEE*, CADEMICS, (Hull, England), pp. 66-71, July 1977.
  [12] M. Glesner and K. Haubrichs, "A new efficient statistical toler-ance analysis and design procedure for electrical networks," *Proc. IEEE*, CADEMICS, (Hull, England), pp. 59-65, July 1977.
  [13] K. H. Leung and R. Spence, "Multiparameter large change sensi-tive package experiment exploration," *IEEE Trans. Circuits*.
- tivity analysis and systematic exploration," IEEE Trans. Circuits Syst., vol. CAS-22, pp. 796-804, Oct. 1975.

- [14] T. R. Scott and T. P. Walker, "Regionalization: A method of pp. 229-234, Apr. 1976. T. B. M. Neill, "Variance reduction in the Monte Carlo analysis of
- [15] electrical networks," Inst. Elec. Eng. Conf. CAD, London, pp. 219-224, Apr. 197
- [16] J. F. Pinel and K. Signhal, "Efficient Monte Carlo computation of circuit yield using importance sampling," IEEE, ISCAS'77, pp. 575-578
- [17] K. S. Tahim and R. Spence, "Statistical circuit analysis-A practi-
- cal algorithm for linear circuits," IEEE, ISCAS'78, pp. 180-184. T. Neumann and D. Agnew, "Tracking sensitivity: a practical [18]
- T. Neumann and D. Agnew, "Tracking sensitivity: a practical algorithm," *Electron. Lett.*, vol. 13, No. 12, pp. 371-372, June 1977. K. S. Tahim, "Statistical analysis and design of electrical [19] networks," Ph.D. thesis, University of London, 1978.



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