The New Future of Design Automation Research

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Semiconductor Research Corporation

July 29, 2009
SIGDA/DAC University Booth
46th Design Automation Conference
San Francisco, California

Semiconductor Research Corporation
A Family of Distinct, Related Program Entities

SRC®

- **GRC** — Global Research Collaboration. Ensuring vitality of current industry
- **FCRP** — Focus Center Research Program. Breaking down barriers to extend CMOS to its limits
- **NRI** — Nanoelectronics Research Initiative. Beyond CMOS – identifying next information element
- **Education Alliance** for Science, Engineering & Technology — Attracting and educating the next generation of innovators and technology leaders
- **TRC(s)** — Topical Research Collaborations. Topic(s) chosen by participants
  - TERC
  - NINE

The Semiconductor Research Corporation's Global Research Collaboration

- SRC-GRC is a not-for-profit consortium of member companies and agencies supporting 540 research tasks at 120 universities worldwide, with 550 faculty investigators, 600 graduate students (including 35 on SRC fellowships/ scholarships), mentored by 600 employees from member companies.

- SRC's employees and industry assignees work with a Board of Directors and technical advisory boards composed of members from participating companies.

global RESEARCH COLLABORATION

2009 University Research Program

Computer-Aided Design and Test Sciences (CADTS)

- Logic and Physical Design
- Test and Testability
- Verification

Integrated Circuit and System Sciences (ICSS)

- Circuit Design
- Integrated Systems Design

Device Sciences (DS)

- Digital CMOS
- Memory Technologies
- Modeling and Simulation
- Compact Modeling
- Analog/Mixed-Signal Devices

Nanomanufacturing Sciences (NMS)

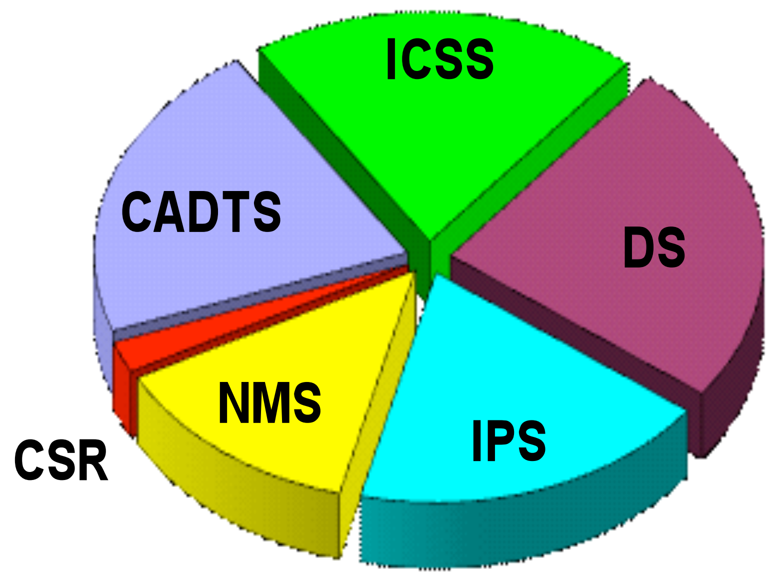
- Patterning
- Factory Systems
- ESH

Interconnect and Packaging Sciences (IPS)

- Packaging
- Back-End Processes

Cross-disciplinary Semiconductor Research (CSR)

- Exploratory grants



SRC-GRC Members and Partners

AMD

IBM

freescale semiconductor

GLOBALFOUNDRIES

Texas Instruments

intel

NOVELLUS

Mentor Graphics

TEL

APPLIED MATERIALS

axcelis

MITRE

ROHM AND HAAS Electronic Materials

cadence

SIA

EPSRC
Engineering and Physical Sciences Research Council

SEMATECH

semi

NIST

NSF

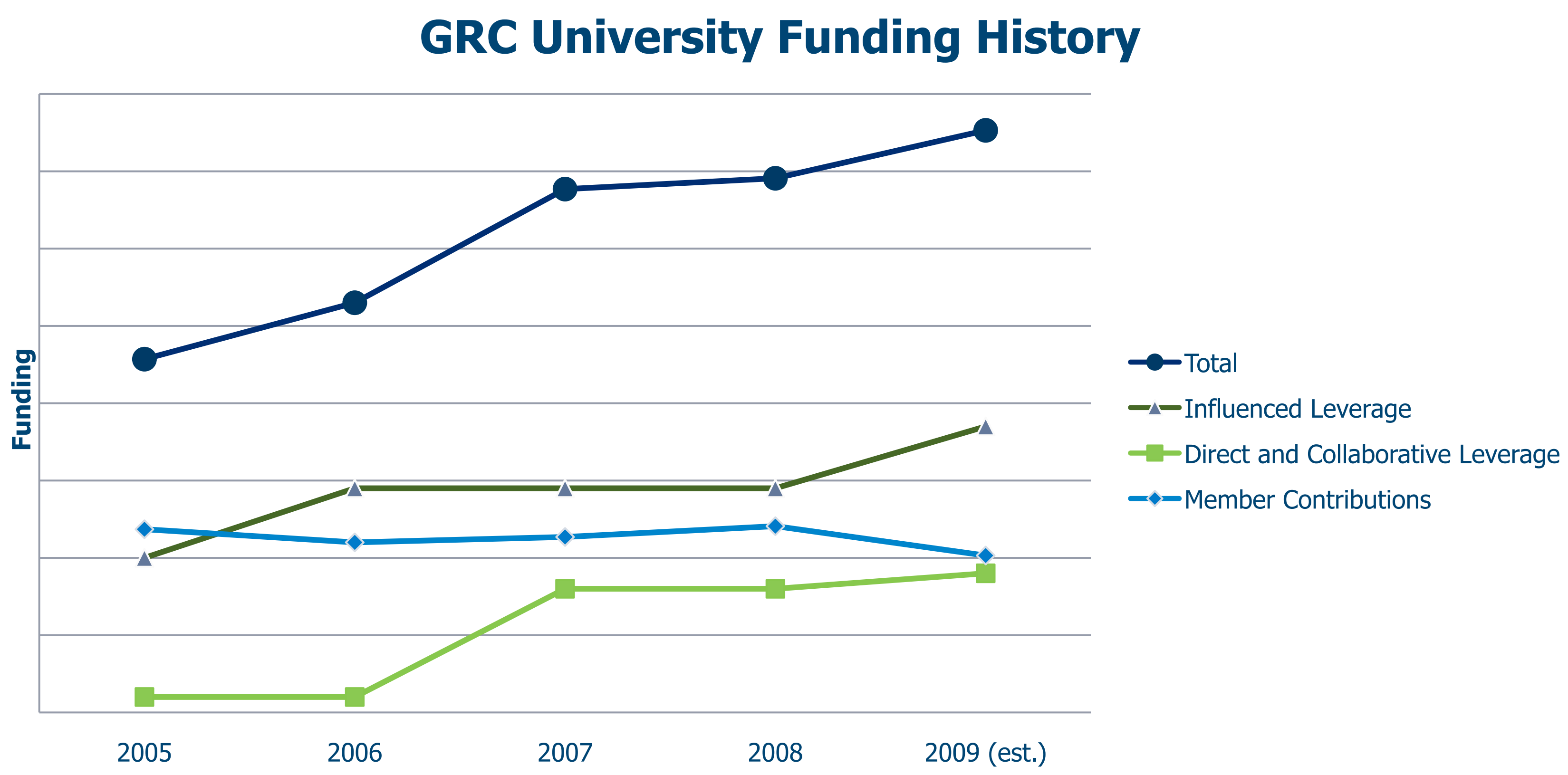
TEXAS Wide Open For Business

georgia.gov

NYSTAR
NEW YORK STATE FOUNDATION FOR SCIENCE, TECHNOLOGY AND INNOVATION

SCIENCE foundation ARIZONA
Innovation at Work

GRC Funding History



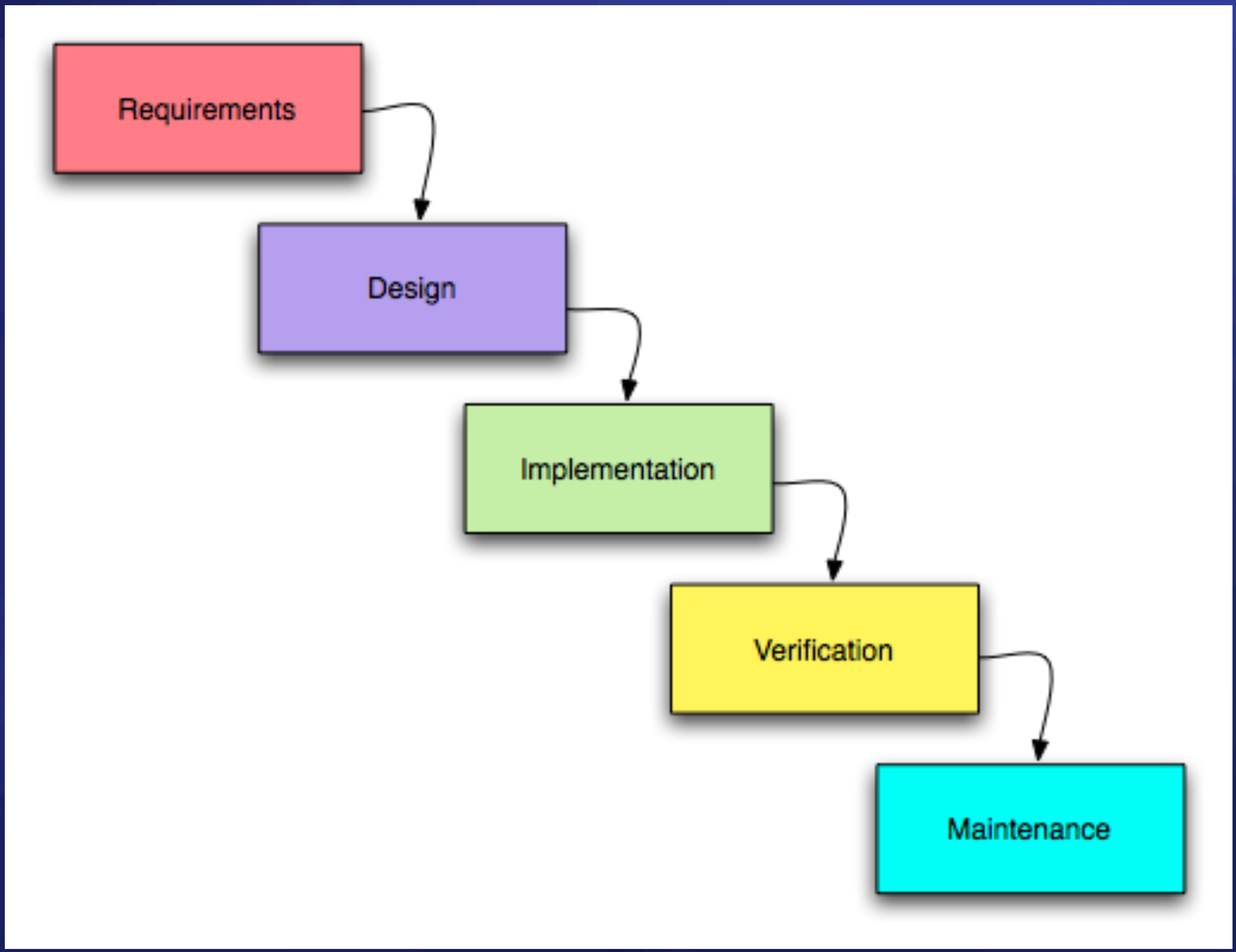
"Brave New World"

"Community, Identity, Stability"

– Aldous Huxley, *Brave New World*, 1932

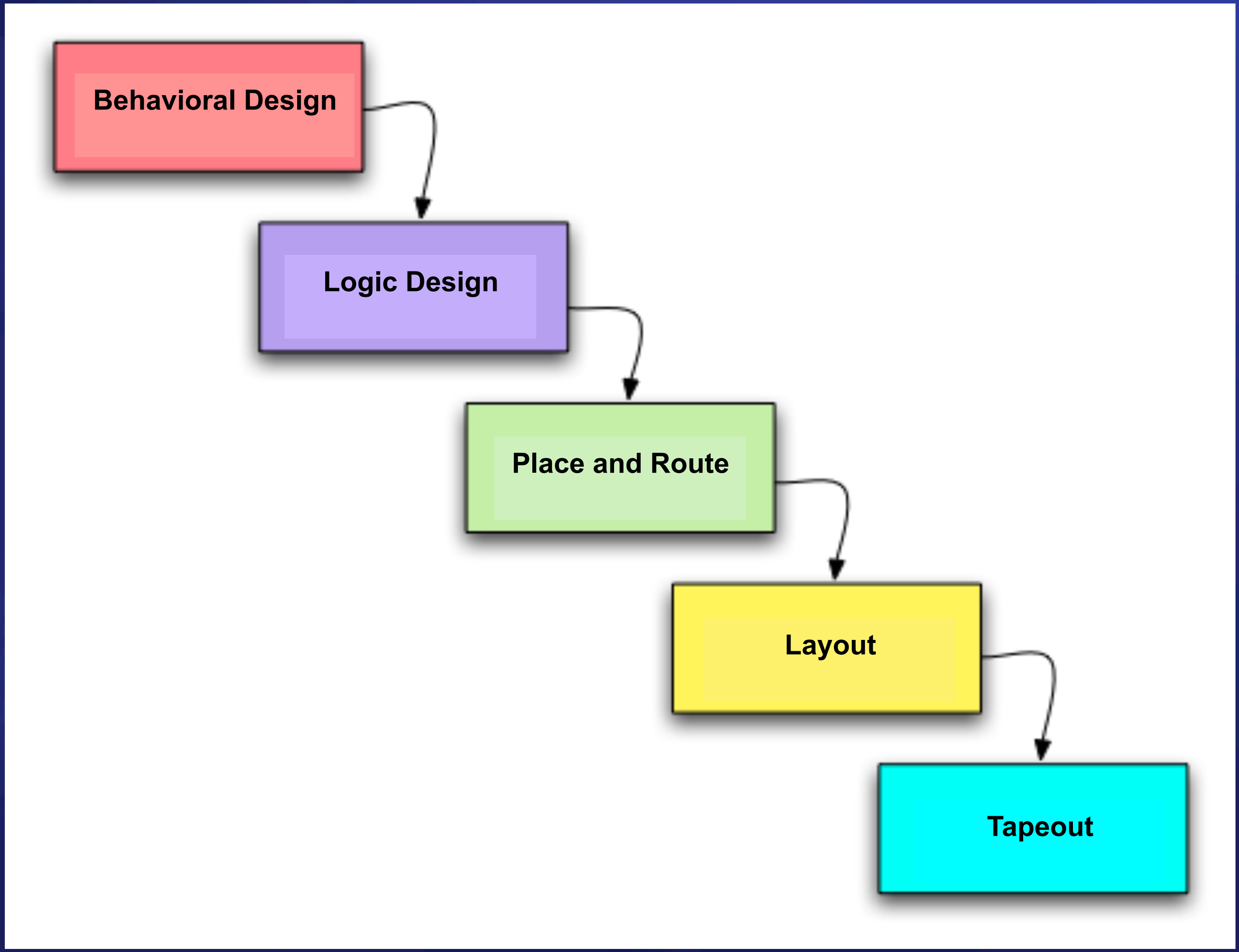
- A **community** of experts from industry and universities, representing multiple disciplines
- Renewed **identity** as an exciting research area
- **Stability** of support for research and education

Old "Waterfall" Chart



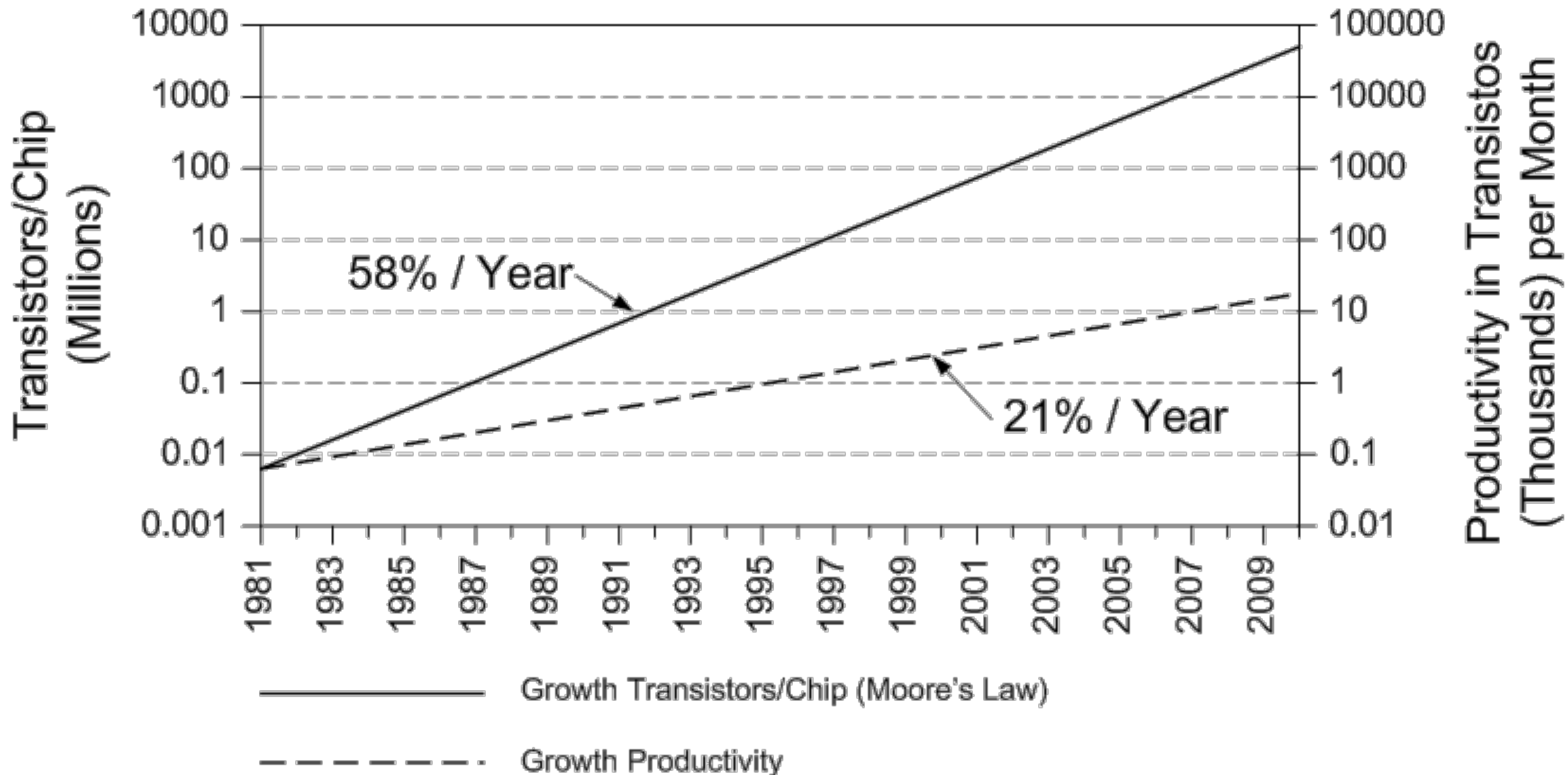
Software

Old “Waterfall” Chart



EDA

Old "Productivity Gap" Chart



Source:
various attributions

Old "Superexponential" Chart

Superexponential Design Complexity

Thousands

\# Transistors

Billions

Functionality + Testability

Functionality + Testability + Wire Delay

Functionality + Testability + Wire Delay + Power Mgmt

Functionality + Testability + Wire Delay + Power Mgmt + Embedded software

Functionality + Testability + Wire Delay + Power Mgmt + Embedded software + Signal Integrity

Functionality + Testability + Wire Delay + Power Mgmt + Embedded software + Signal Integrity + Hybrid Chips

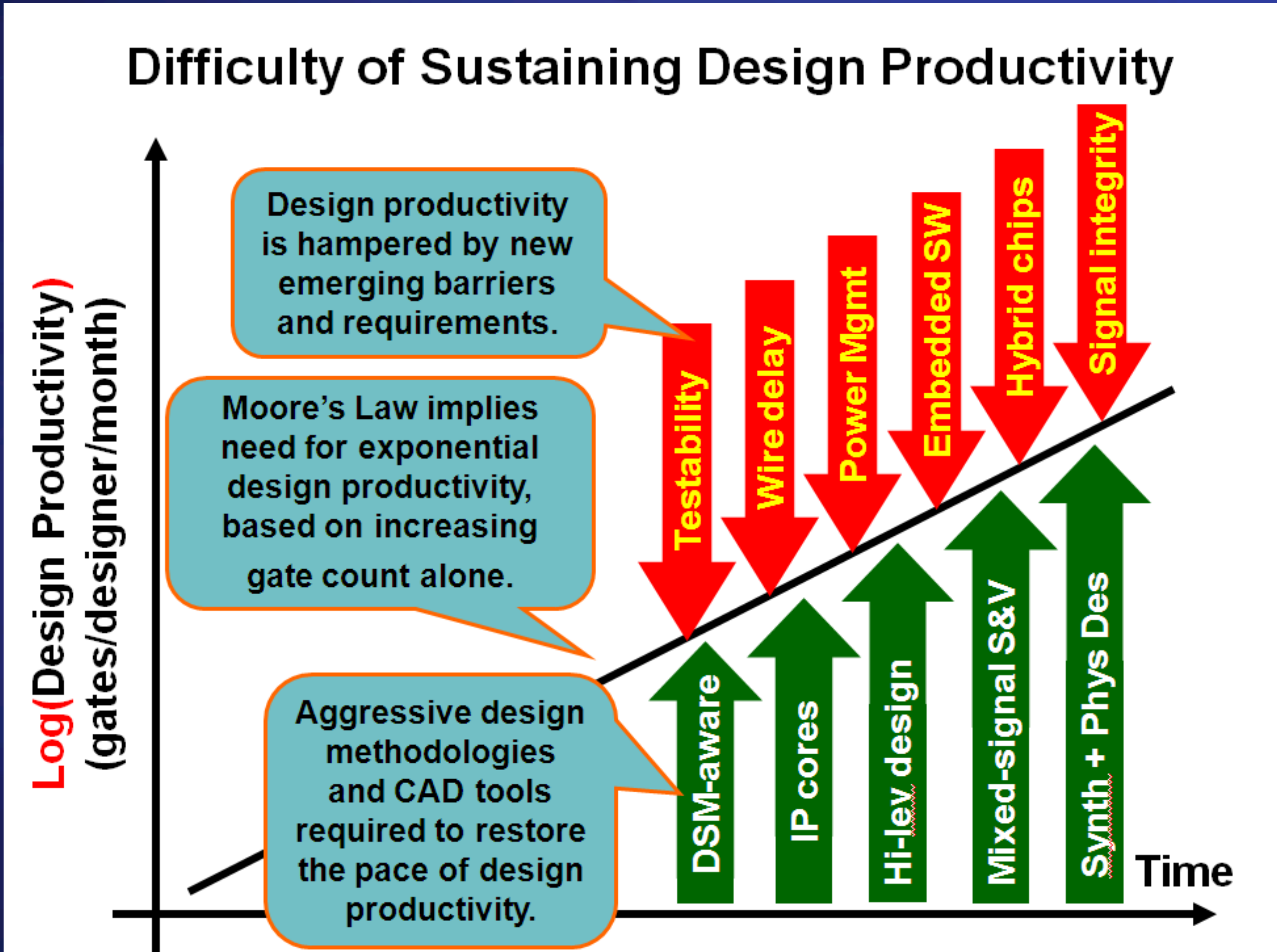
Functionality + Testability + Wire Delay + Power Mgmt + Embedded software + Signal Integrity + Hybrid Chips + RF

Functionality + Testability + Wire Delay + Power Mgmt + Embedded software + Signal Integrity + Hybrid Chips + RF + Packaging

Functionality + Testability + Wire Delay + Power Mgmt + Embedded software + Signal Integrity + Hybrid Chips + RF + Packaging + Mgmt of Physical Limits

- ✓ Exponentially growing number of elements (devices & wires)
- ✓ Design complexity is exponential function of element count

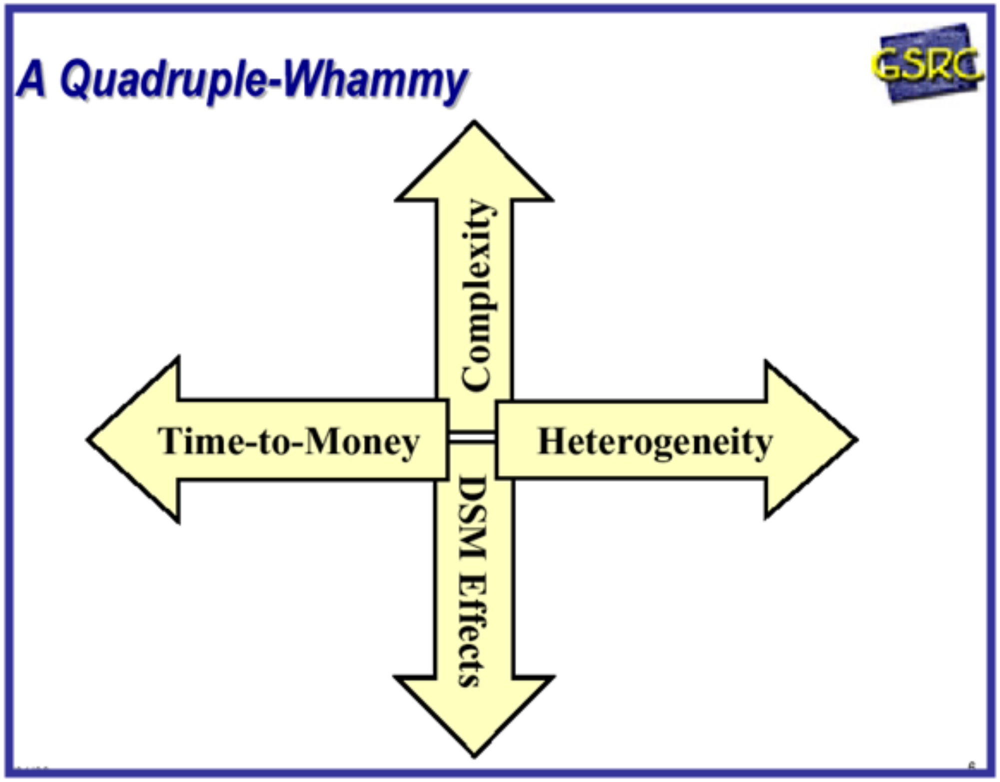
Old “Wilting Rod” Chart



Old “Quadruple Whammy” Chart

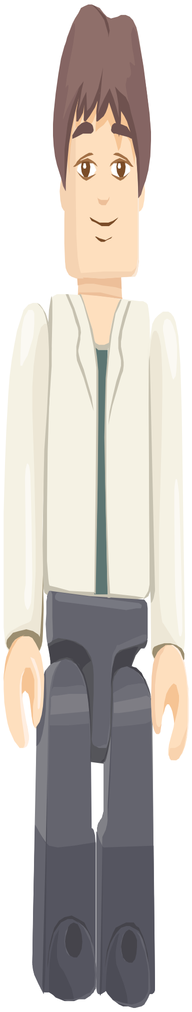
“Quadruple Whammy” for Design and Tools

- Design of each transistor and wires harder
- Exponentially more transistors
- More elements doing different things
- Greater design risk, greater variety, and smaller design window

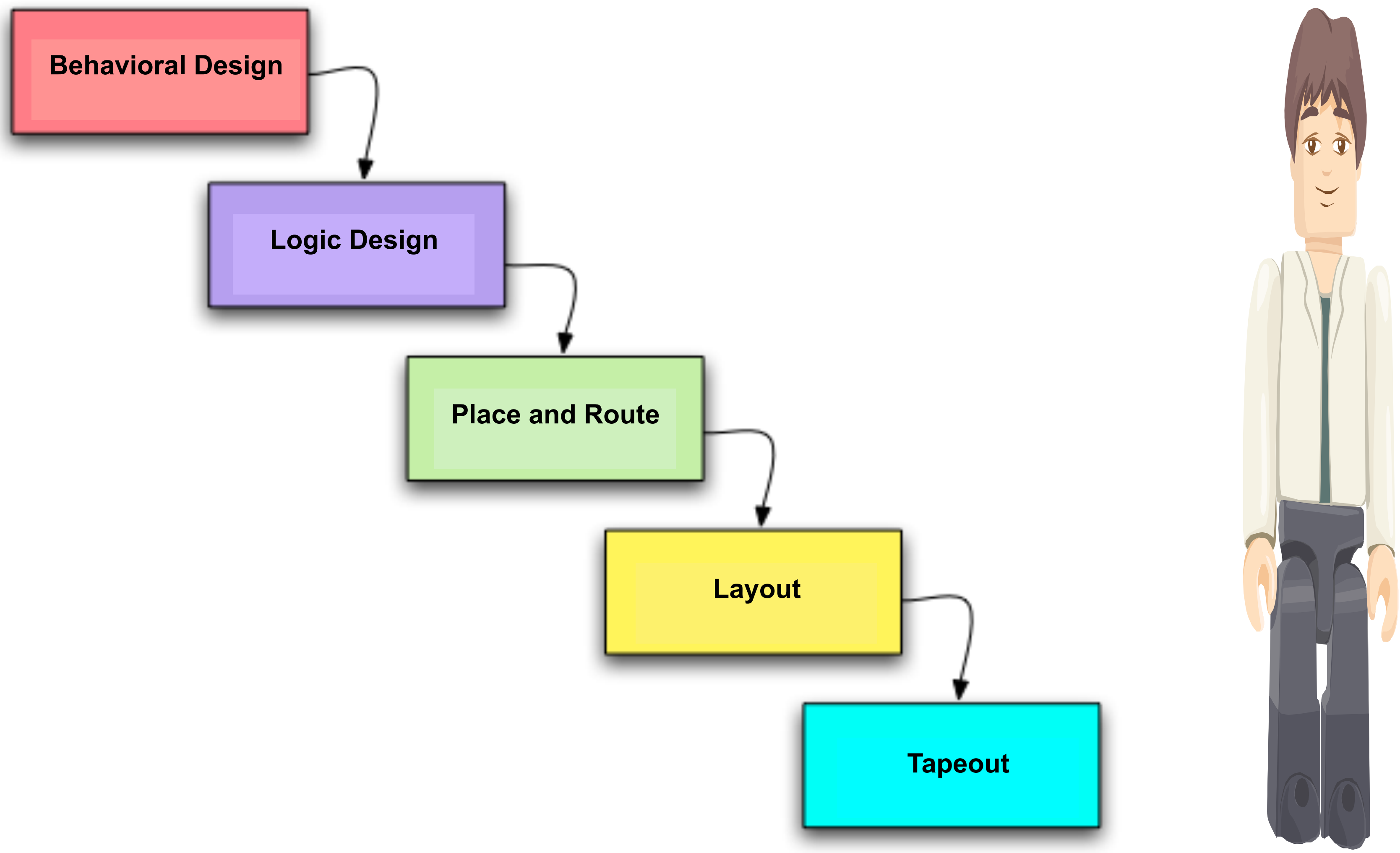


Source: Kurt Keutzer
20^{th} century

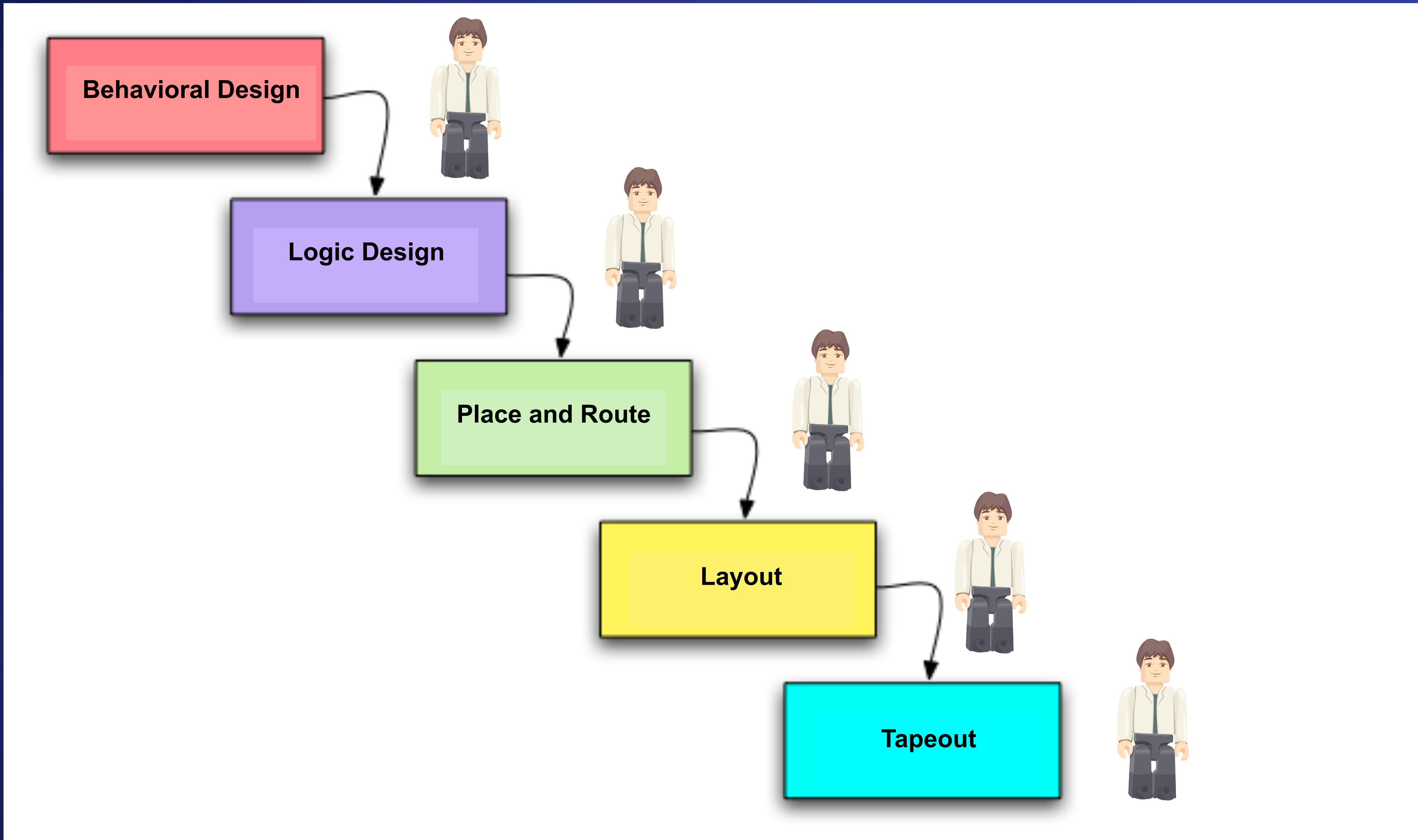
Tall Thin Designers



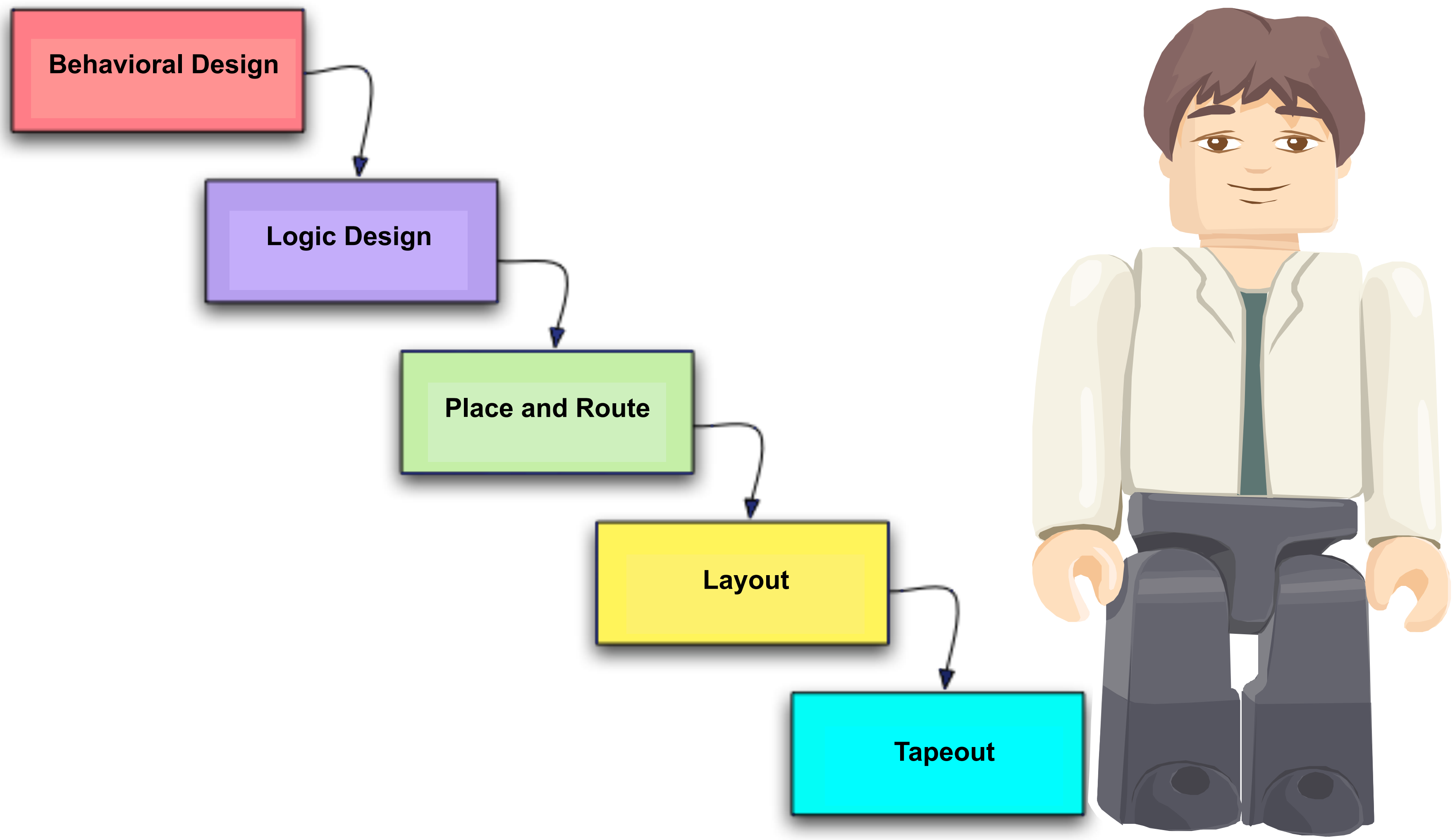
Tall Thin Designers



Short Thin Designers



Tall Fat Designers



Foundations of Computer Science

FOCS 2008

1/78 in circuit and logic design/minimization

FOCS 1960, 1961

30/33 in circuit and logic design/minimization

Muroga, Akers, Roth, McCluskey, Karp, . . .

FOCS 2009

50th Annual IEEE Symposium on Foundations of Computer Science

October 24-27, 2009

Atlanta, GA

IEEE COMPUTER SOCIETY

Examples of the research articles in semiconductors that resulted in Nobel Prizes

Article	Nobel Prize		# of citations	
	in:	for:	25 years from publication	through 2008
Bardeen J, Brattain WH "The Transistor, a Semi-conductor Triode", Phys. Rev. 74 (2): 230-231 1948	1956	Discovery of semiconductor transistor	**71**	**235**
Esaki L, "New Phenomenon in Narrow Germanium p-n Junctions", Phys. Rev. 109 (1958) 603	1973	Discovery of tunnel diode	**247**	**547**
Kroemer H, "Heterostructure Bipolar-transistors and Integrated-circuits", Proc. of the IEEE 70 (1982) 13	2000	Invention of heterojunctions	**577**	**609**

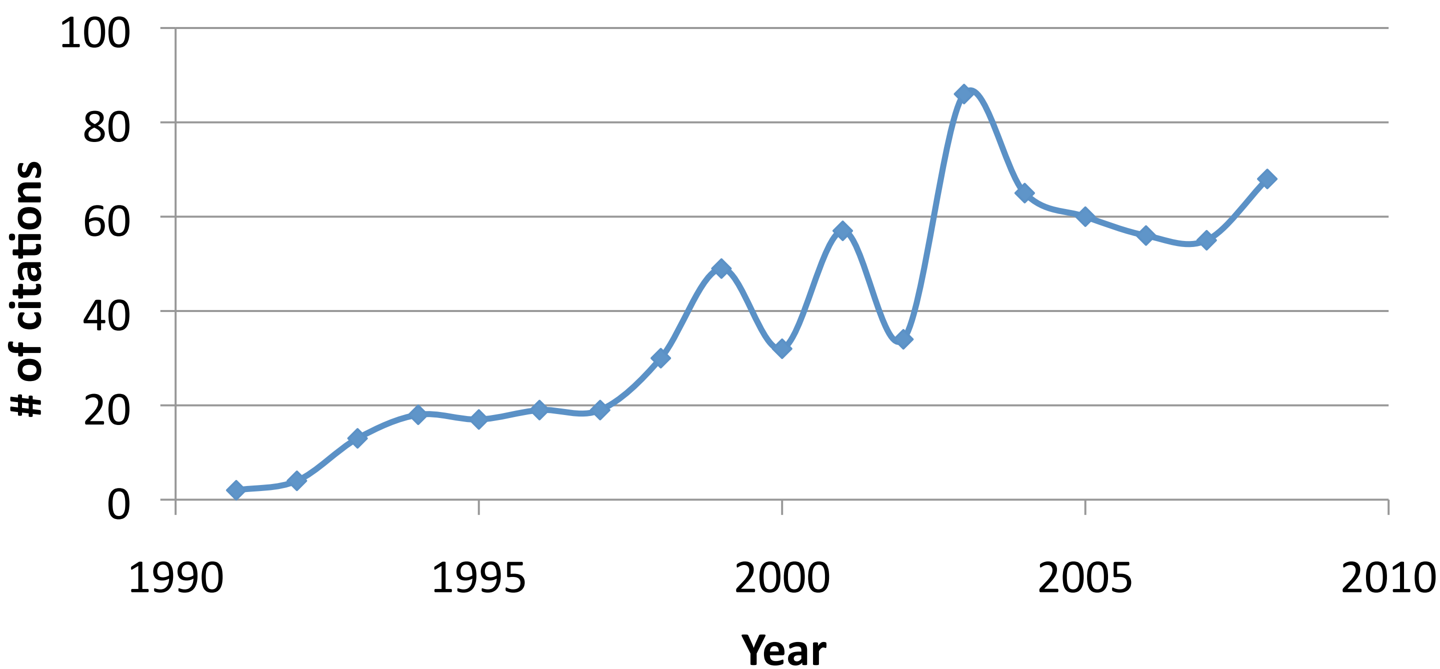
Source: Victor Zhirnov, SRC

Publication Lifetime*

Example: **Design/CADTS**

"Asymptotic Waveform Evaluation for Timing Analysis", by Pileggi and Rohrer, IEEE Trans. Computer-Aided Design 9 (4)352 (1990)

677 citations **188 citations by industry (28%)**



*Average lifetime is 5 years

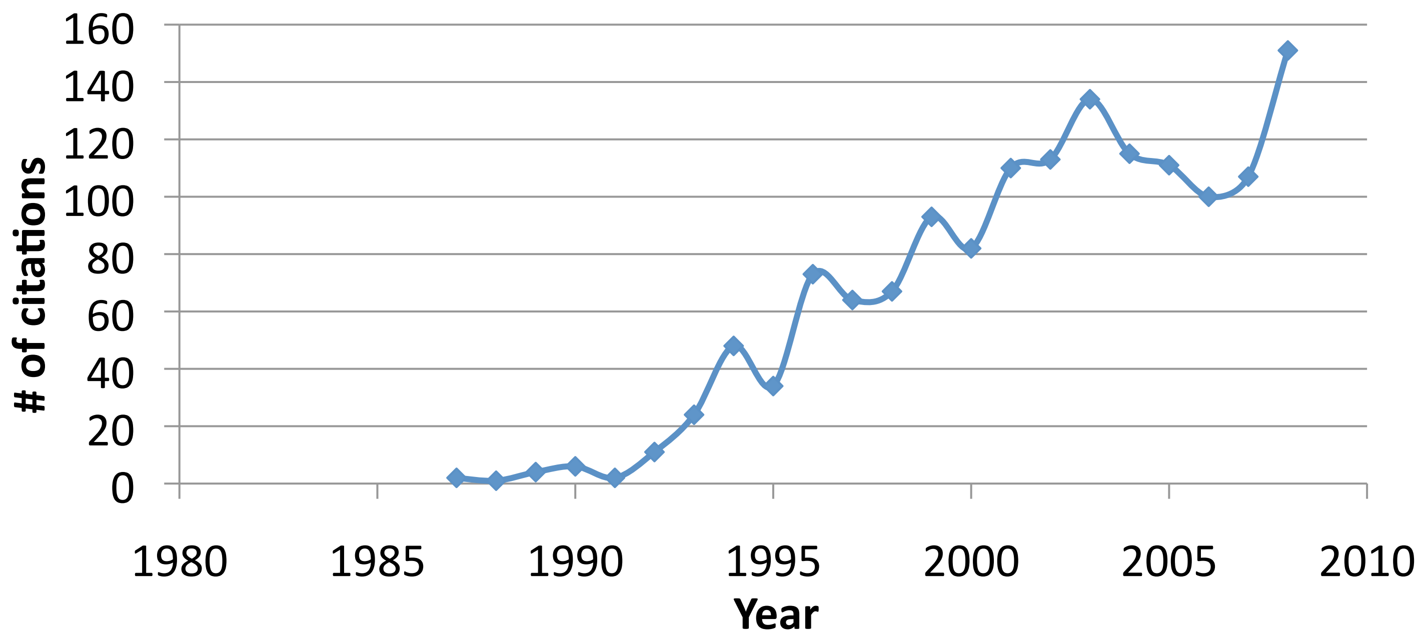
Source: Victor Zhirnov, SRC

Publication Lifetime*

Example: **Design/CADTS**

"Graph-based Algorithms for Boolean Function Manipulation" by R. E. Bryant, IEEE Trans. Computers 35 (8): 677 (1986)

1443 citations **283 citations by industry (25%)**



*Average lifetime is 5 years

Source: Victor Zhirnov, SRC

Three Grand Challenges in Design Automation

Challenges in design automation are many, but they can be grouped into three areas:

- **System-level design** is needed at the top to increase the productivity of designers – otherwise efficient use cannot be made of advanced devices and materials

- **Robust optimization** in the middle is necessary to contain the exploding complexity of systems and to offset the diminishing returns afforded by feature size shrinkage

- **Design for manufacturing** at the back end (and throughout the flow) is critical to assure that we can produce products using new technologies

Models and **abstractions** are key at all levels of the design process

Source: 2006 NSF Forum

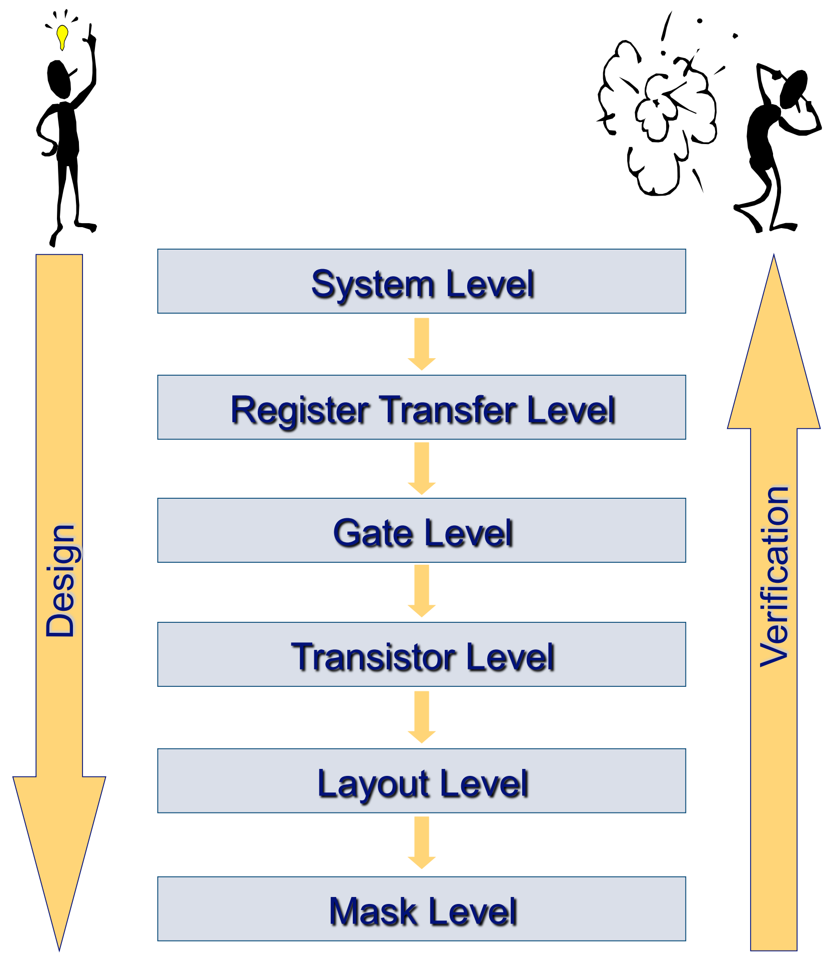
System-Level Challenges

- **System level** techniques are needed to achieve shorter design times with higher quality to address system level problems: clock, power management, interconnection, fault tolerance, …
- Design tools must extend to where design is going, including the **software level**
- A **compositional method** of designing and connecting modules such that the functionality and performance are predictable is needed; it must be aware of implementability, verification, test, and reliability
- A design flow and methodology must enable more sophisticated handoffs; a **collaborative framework** must focus on the interfaces between abstraction levels to allow stable robust, reusable design IP
- We must be able to implement **hybrid systems** efficiently - model, explore, design, optimize, and integrate non-digital functionality (MEMS, NEMS, analog/RF, sensors/transducers, photonics, biological, …)

Source: 2006 NSF Forum

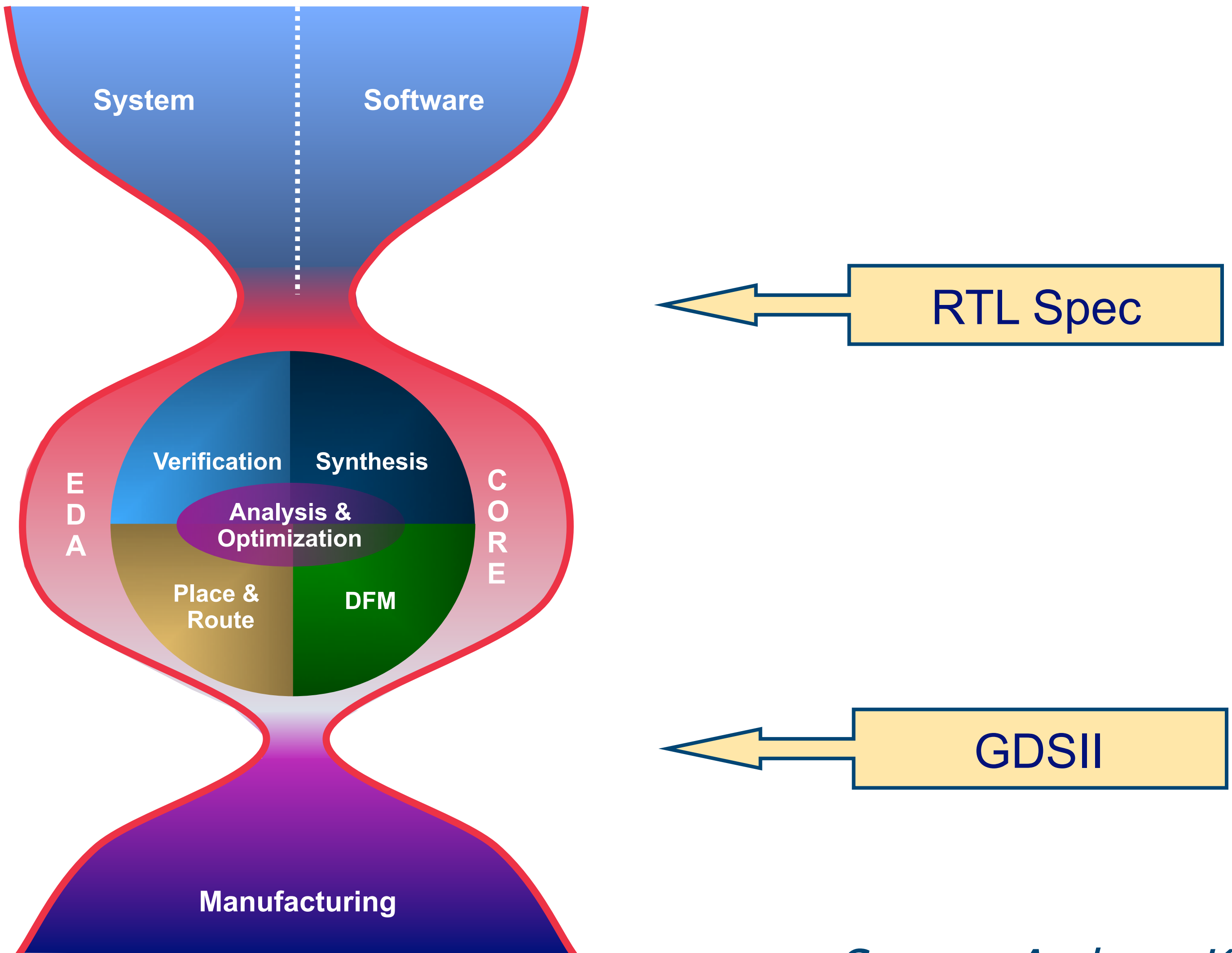
Ever Increasing Design Flow Complexity

- Expansion of traditional RTL-to-layout DA support
  - Upwards: System specification, transaction level modeling, behavioral synthesis
  - Downwards: RET, OPC, yield optimization through post-layout manipulations, etc.
  - In between: more and more complex optimizations



Source: Andreas Kuehlmann 2006 NSF Forum

Most of Design Automation Today Focuses on the "Middle"



Source: Andreas Kuehlmann
2006 NSF Forum

Optimization Challenges

- Optimization algorithms must be what many of today's design automation techniques are not: **stable, scaleable,** and **robust**
- Design automation must **leverage optimization technology** – casting problems in optimization terms opens a new resource of partnerships in cross-disciplinary research that can lead to better optimization engines
- Optimization algorithms need to handle **multiple objectives** simultaneously to address critical power, variability, manufacturability,
- Techniques must **globally optimize performance** across layers of abstraction and diverse technologies

Source: 2006 NSF Forum

Technology/Manufacturing Challenges

- Design for manufacturing must move from handling variability to **robust operation in the face of failures** from multiple sources
- Design tools must **comprehend multiple options** associated with new devices, new materials, fabrics and 3D stacking
- Communication between layout/design must go beyond sets of rules to **process/manufacturing understanding at all levels**.
- Tools must comprehend **hybrid devices** and **materials** as well as **emerging nontraditional applications** (bio, sensor, medical, etc.)
- Design techniques addressing these **late-CMOS technology challenges** must bridge to beyond-CMOS nanotechnologies as well

Source: 2006 NSF Forum

Recommendations

- Since design automation is critical to advancing our computing capability for the 21st century:
  - NSF should support a **collaborative platform** for design automation research pushing towards beyond-CMOS technologies
  - NSF must establish and support multidisciplinary **partnerships** to enable the design technology work necessary for 21st century leadership:
  - ✓ enabling **system-level design** in partnership with the software and architecture areas
  - ✓ with larger-scale, more robust **optimization** to provide more complex systems and keep on Moore's Law pace
  - ✓ at the **nanoscale** to take design technology from novel devices to system-level applications

Source: 2006 NSF Forum

Why Should NSF Worry about Design Technology?

- **Design will be a key differentiator for US competitiveness and national security.**
  - US must have the most productive designers
  - Design costs dominate – they need to be dramatically reduced in terms of team size, design time, etc. to maintain US lead
- **National support for design research is diminishing in US, increasing elsewhere.**
  - China, Europe, Taiwan, and Canada all support university-based design research infrastructure
  - National strategy in design needs to match national investment in materials and technologies
  - Education funding must help supply trained scientists and engineers
- **Moore's Law is a critical enabler for advances in computing and its future depends on design**
  - Materials and process technology alone cannot keep us on the Moore's Law curve.
  - Advanced applications – DNA sequencing, astrophysics, cryptography – rest on this computational foundation

Source: 2006 NSF Forum

The 2006 Forum – A Report Card

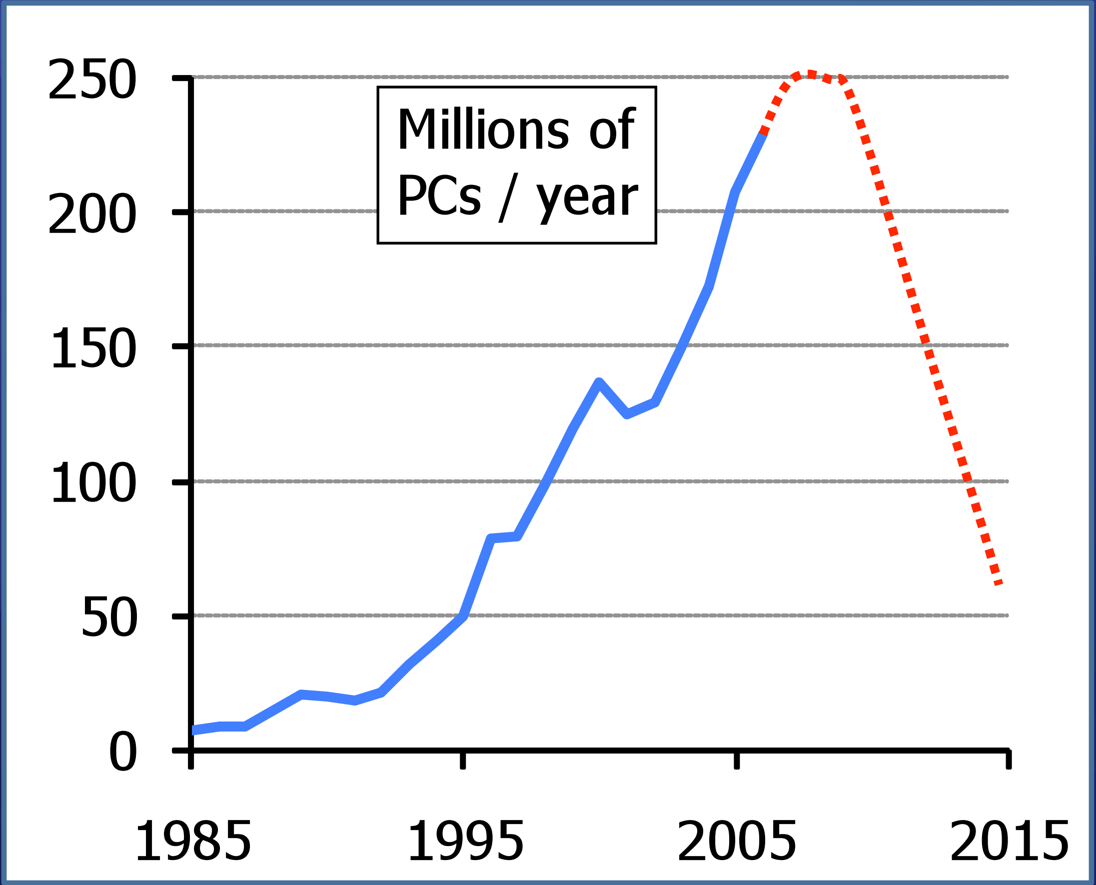
A **National Design Initiative** (NDI)		INC
System design science	INC	
Robust optimization methodologies	B	
Interface to manufacturing	B	
Collaborative research framework:		INC
Access to **leading edge fabrication technologies**	C	
A **computational discovery environment**	?	
Opportunities for **design of innovative integrated electronic systems**	INC	
$50M per year for five years through a cross-directorate initiative by NSF		INC

What's New (Well, Not Really New)

- New emphasis on parallelism
- New ITRS design and software emphasis
- New focus on applications
- New post-CMOS technologies
- New (old) predictions about the death of EDA

The Sequential Peril

Cores not faster +
no parallel improvement
→ SW not faster
→ no new PC sales
except for wearout
→ sales drop 250M
↓
50M



Source: Dave Patterson, SRC, 2004

SRC/NSF Joint Program on Multicore Design and Architecture

- Joint needs development, solicitation, and selection of projects in multi-core architecture, design, tools, and interconnect
- $10M, 3-year program
- 28 new tasks from 27 universities with 43 faculty (including 17 new investigators and 7 former SRC students) selected for 8/09 starts

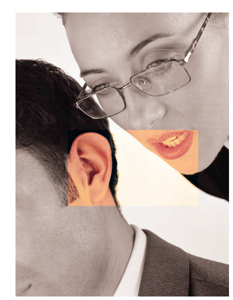
New Emphases in 2008 ITRS

- Importance of **software as an integral part of semiconductor products**
- **Software design productivity** as a key driver of overall design productivity
- Heavy use of special purpose **multi-core architectures** as a key enabler of productivity growth
- Continued emphasis on **system-level design**
- Special section on **energy**
- New term ***Design Equivalent Scaling*** refers to design technologies that enable high performance, low power, high reliability, low cost, and high design productivity.

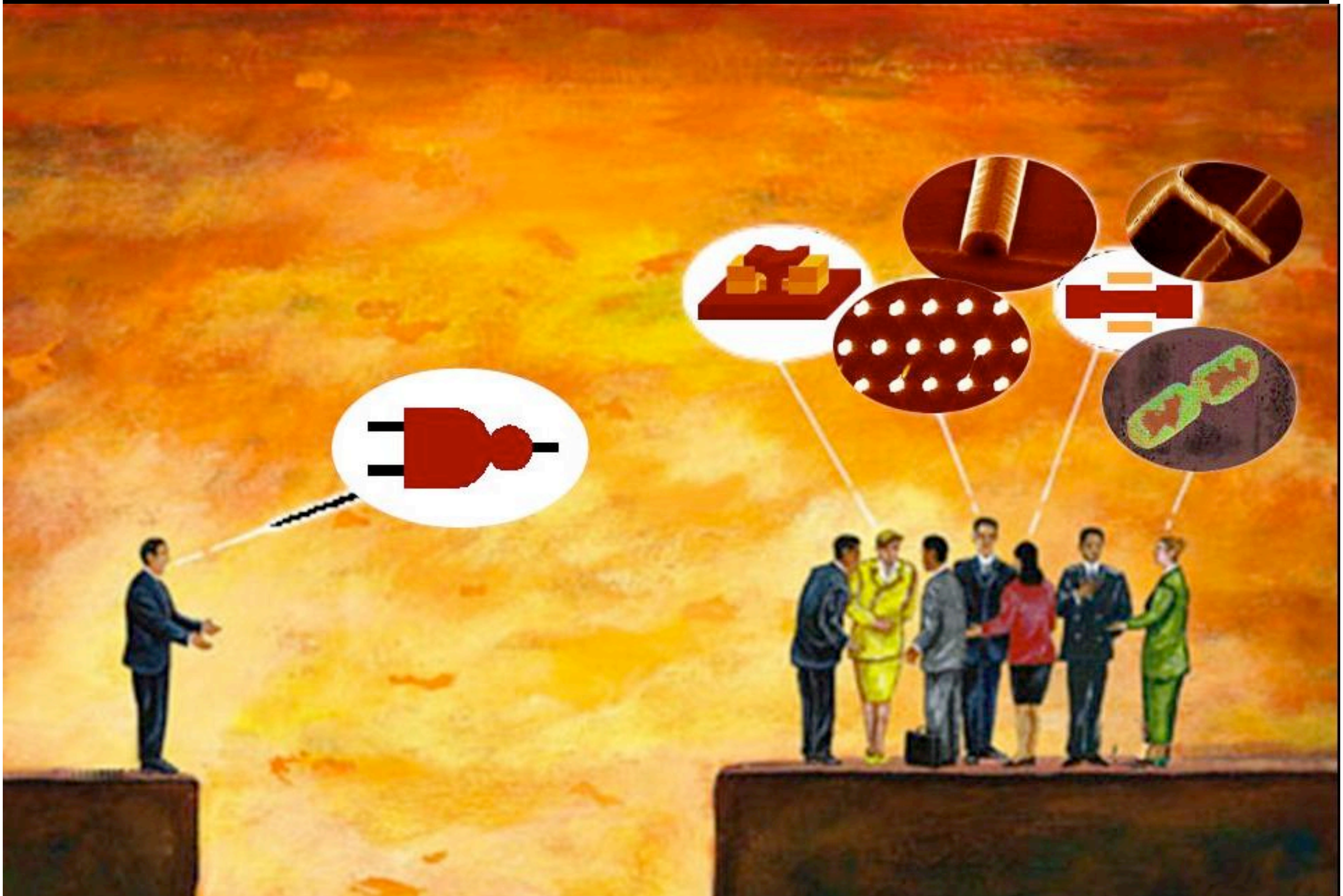
ITRS International Technology Roadmap for Semiconductors

Compelling Laptop/Handheld Apps

- Health Coach
  - Since laptop/handheld always with you, Record images of all meals, weigh plate before and after, analyze calories consumed so far
    - "What if I order a pizza for my next meal? A salad?"
  - Since laptop/handheld always with you, record amount of exercise so far, show how body would look if maintain this exercise and diet pattern next 3 months
    - "What would I look like if I regularly run 2 miles? 4 miles?"
- Face Recognizer/Name Whisperer
  - Laptop/handheld scans faces, matches image database, whispers name in ear (relies on Content Based Image Retreival)

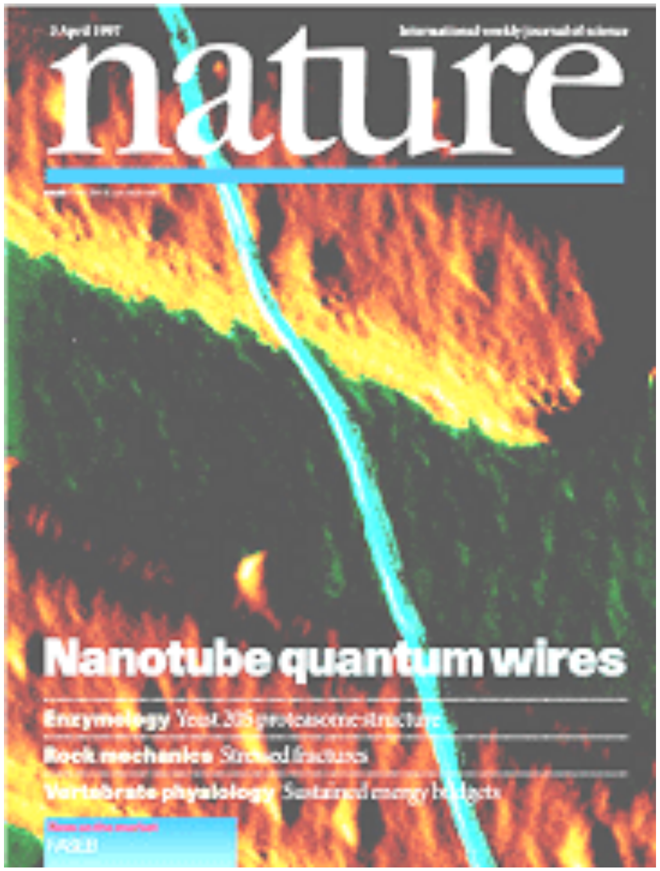


Source: Dave Patterson, SRC, 2004



Source: Rob Rutenbar

Ultimate Measures of Success . . .



For the *technologist*:

I/V curve in *Nature*

For the *circuit designer*:

Best Paper Award at ISSCC

(Rob Rutenbar, 2004)

Algorithms, Coding, Logic, Architectures, Applications

Key question: Will the behavior of nanodevices be so strange that our "higher level" abstractions need to change?

Key answers:

NO, a switch is a switch

YES, that's the whole idea

NRI 2009
Architecture Benchmarking Exercise

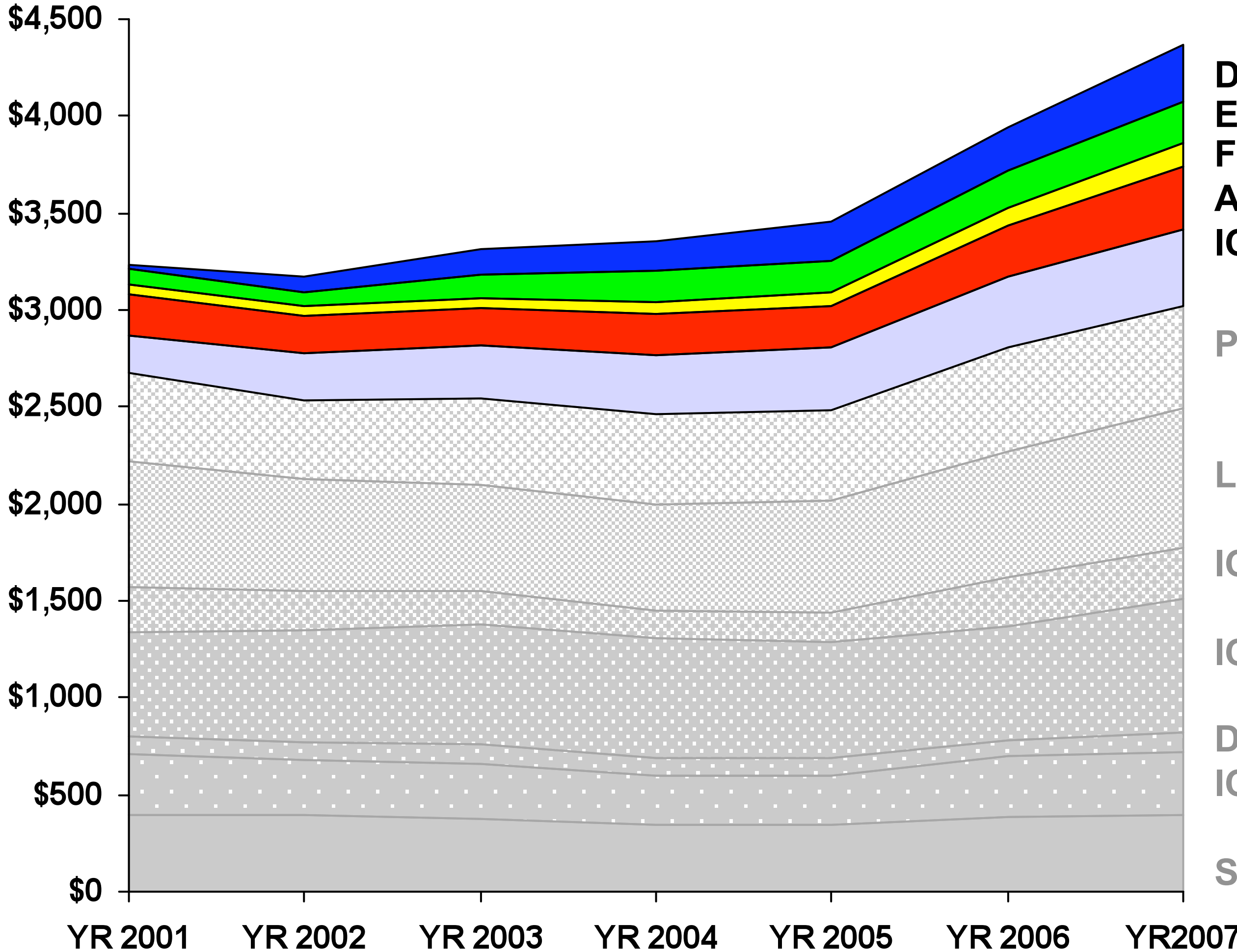
Magnetic Tunnel Junction	Markovic	UCLA	WIN
Spin Wave Devices	Khitun	UCLA	WIN
Mag Dot Logic	Roychowdhury	UCLA	WIN
BiSFET	Register	UT	SWAN
Graphene Veselago Devices	Lee	SUNY	INDEX
Excitons	Baldo	MIT	INDEX
Magnetic Rings	Ross	MIT	INDEX
Tunnel FETs	Seabaugh	ND	MIND
Nanomagnet logic	Niemier	ND	MIND
Plasmonic logic	Mazumder	Michigan	MIND
Graphene thermal logic	Chen	Purdue	MIND
Graphene spin transport	Ye	Purdue	MIND
Binary Decision Diagram Arch	Datta	PSU	MIND
Multiferroic based devices	Salahuddin	UCB	WIN

EDA Myths and Realities in 2009

- EDA is entering a mature phase
  EDA growth opportunities come from solving new problems
- Adoption of new technology is slowing
  Adoption of leading-edge semiconductor technology is the same rate as in the past
- Once an EDA market stabilizes, there is no opportunity for change
  Even in low-growth markets, technical discontinuities create opportunities for market share changes
- Companies can't afford the growing cost of EDA
  EDA cost is decreasing at the same rate as semiconductor manufacturing cost
- Companies are consolidating around single vendor platforms
  Companies are increasingly moving toward best-in-class design sub-flows
- Semiconductor industry is consolidating
  Semiconductor industry has not been consolidating

Source: Wally Rhines, DesignCon 2009

New Methodologies Drive EDA Revenue Growth



5-YR CAGR

DFM* …….…………… 33%
ESL ……………..……… 24%
Formal ………………… 20%
A/MS & RF ……………. 11%
IC/ASIC Analysis ……. 10%

PCB Design …………… 5%

Logic Verification ……... 5%

IC Full Custom …………. 4%

IC Place & Route ………. 4%

DFT ……………………..….. 3%
IC Verification ………..…. 2%

Synthesis/Capture …….. 0%

EDAC Market Statistics Service
** DFM Includes DFM, RET, Mask Data Prep & TCAD*

Source: Wally Rhines, DesignCon 2009

What Next

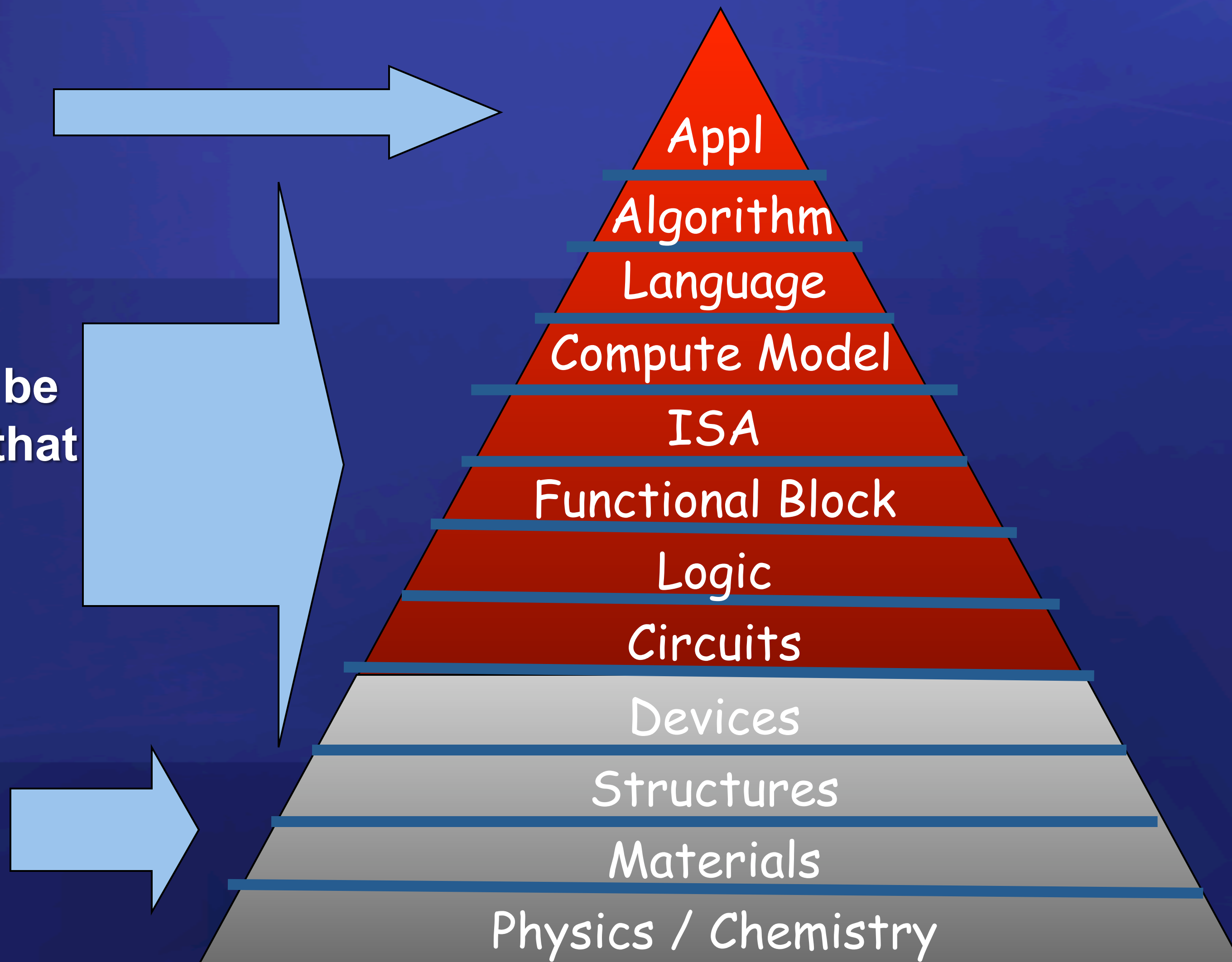
- A **community** of experts from industry and universities, representing multiple disciplines
- Renewed **identity** as an exciting research area
- **Stability** of support for research and education

The Food Pyramid

There needs to be pull from up here

And there need to be models and tools that connect them

There is much investment and bottom-up work here



Source: Rob Rutenbar

What Next

- Strengthen the links between theory of computation and design automation
- Maintain strong industry/university/government partnerships
- Grow support for design and design automation as increasingly important contributors to the roadmap forward

What Professional Societies Do to Support the New Future of Design Automation Research

- Conference sponsorship: DAC, ICCAD, DATE, ASP-DAC, . . .
- Publications: TODAES, TCAD, ESL, newsletters, . . .
- Awards: Dissertation, New Faculty, Newton, McCalla, Fellows, . . .
- Events: University Booth, Ph.D. Forum, workshops, speakers, . . .
- Fellowships, grants, . . .

What You Can Do

- Do research
- Support research
- Contribute to publications
- Read publications
- Come to conferences and workshops and interact
- Join and support professional societies

Be a part of the new future of design automation research!

THANK YOU!