2009 SIGDA University Booth at DAC Program

http://www.sigda.org/programs/UniversityBooth/Ubooth2009/

1. **Chung Cheng University:** Design and Implement a Reliable Multicore Debugging Framework.
2. **Dresden University of Technology:** A Heterogeneous MPSOC with Hardware Supported Dynamic Task Scheduling for Software Defined Radio.
3. **Drexel University:** Post-CTS Delay Insertion.
4. **Hanyang University:** Simultaneous Mapping and Scheduling for Multi-core Systems, by Using Iterative Zone Refinement.
5. **Hanyang University:** Effective Techniques for Low Cost Post-Silicon Repair.
6. **Iowa State University:** Securing the integrated circuit supply chain: an efficient and effective reconfigurable keying of integrated circuits for intellectual property protection.
7. **Lafayette College:** Visualization Aides for Computer Architecture Education.
8. **Nagoya University:** Advanced SystemBuilder: A System-Level Design Toolkit.
9. **National Cheng Kung University:** A Two-Stage ILP-Based Droplet Routing Algorithm for Pin-Constrained Digital Microfluidic Biochips.
10. **National Cheng Kung University:** Process Variation Aware Clock Network Synthesis for Low Power SoC Design.
11. **National Sun Yat-Sen University:** Hardware/Software Co-debugging and Real-Time Performance Monitoring Platform for 3D Graphics SoC Development.
12. **National Taiwan University:** Qute Virtual Platform (QuteVP): A Multi-Million-Instructions-per-Second and Cycle-Count-Accurate Virtual Platform for SoC Hardware/Software Co-Design.
13. **Polytechnic Institute of NYU:** Security of JTAG.
14. **Seoul National University:** ePRO-MP, for profiling and optimizing energy and performance of mobile multithreaded applications.
15. **Seoul National University:** HOPES: A Retargetable Parallel Programming Environment for MPSoC.
16. **Seoul National University:** Open source cycle-accurate system-level energy and timing simulator capable of simulating bus cycle level behaviors of an AMBA based system.
17. **Seoul National University:** MPSOC H/W and compiler for video codec.
18. **Seoul National University:** Chip implementation of coarse-grained reconfigurable architecture which supports floating-point operations by co-operation of a couple of integer processing elements.
19. **Tokyo Institute of Technology:** Tightly Coupled Thread Model Based Multiprocessor System on Chip design Framework.
20. **UFRGS:** A clock mesh design space exploration tool.
21. **UFRGS:** SwitchCraft – A tool for switch network generation.
22. **Univ. of New South Wales:** Provably correct on-chip communication: A formal approach to automatic protocol converter synthesis.
23. **Univ. of Texas at Austin:** Low power high performance CAD for on-chip nanophotonic interconnect solution of future Chip-Multi Processors.
24. **University of California, Santa Cruz:** Teaching VLSI Design in 10 Weeks.
25. **University of California, Santa Cruz:** Fast Thermal Aware Floorplanning.
26. **University of Erlangen-Nuremberg:** System-level Design of Heterogeneous Automotive Networks.
27. **University of Erlangen-Nuremberg:** Dependability-Aware System Synthesis using SystemCoDesigner and JReliability.
28. **University of Illinois, Urbana-Champaign:** Workload Adaptive Shared Memory Multicore Processors with Reconfigurable Interconnects.
29. **University of Illinois, Urbana-Champaign / University of California, Los Angeles:** FCUDA: Enabling Efficient Compilation of CUDA Kernels onto FPGAs.
30. **University of Lugano:** A Design Flow and Evaluation Framework for DPA resistant instruction set extension.
31. **University of Pittsburgh:** ACME: An Architecture Compiler for Model Emulation.
32. **University of Tokyo:** System-level debugging, verification and analysis using FLEC.
33. **Universtity of Potsdam:** Synthesis of Adaptive Multiprocessor on Chip within the PinHaT-Tool.
34. **Virginia Tech:** Circuit-Level Techniques for Reliable Physically Uncloneable Functions.
35. **Budapest University of Technology and Economics:** LOGSYS educational tools.
36. **University of Genoa:** From Gates to Embedded Systems with DEEDS: a Bottom-up Approach to Digital Design.

Demo Schedule

	Monday	Tuesday	Wednesday	Thursday
9:00-10:00	Demo Group1	Demo Group 3	Demo Group 1	Demo Group 3
10:00-11:00				
11:00-12:00	Demo Group 2	Demo Group 4	Demo Group 2	Demo Group 5
12:00-1:00				
1:00-2:00	MSE Demo Group		Keynote Speaker	
2:00-3:00		Demo Group 5		
3:00-4:00			Demo Group 4	
4:00-5:00		Social	Social	
5:00-6:00	Social			

Demo Group 1 consists of Demo 8 at Station #1, Demo 14 at Station #2, Demo 16 at Station #3, Demo 15 at Station #4, Demo 17 at Station #5, and Demo 26 at Station #6.

Demo Group 2 consists of Demo 1 at Station #1, Demo 2 at Station #2, Demo 4 at Station #3, Demo 25 at Station #4, Demo 12 at Station #5, and Demo 19 at Station #6.

Demo Group 3 consists of Demo 30 at Station #1, Demo 22 at Station #2, Demo 5 at Station #3, Demo 27 at Station #4, Demo 33 at Station #5, and Demo 34 at Station #6.

Demo Group 4 consists of Demo 20 at Station #1, Demo 6 at Station #2, Demo 10 at Station #3, Demo 21 at Station #4, Demo 23 at Station #5, and Demo 28 at Station #6.

Demo Group 5 consists of Demo 13 at Station #1, Demo 18 at Station #2, Demo 29 at Station #3, Demo 11 at Station #4, Demo 32 at Station #5, and Demo 9 at Station #6.

The MSE Demo Group consists of Demo 7 at Station #1, Demo 24 at Station #2, Demo 31 at Station #3, Demo 3 at Station #4, Demo 35 at Station #5, and Demo 36 at Station #6.