Automatic Generation of Hierarchical Placement Rules for Analog Integrated Circuits

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Overview

• Motivation: analog placement constraints
• Generation of hierarchical placement rules
• Experimental results
  – Comparison with industrial tool
  – Fully differential amplifier
• Conclusion
Constraints in Design Flow

specification

structure

sizing

placement

routing

analog block

sizing constraints

placement constraints

routing constraints

process variations, parasitic devices etc.

manual

mostly automated

mostly manual

mostly automated
Placement Constraints – Device Matching

- Device matching: equal electrical properties
- Sources of mismatch, e.g.,
  - Distance effects
    (temperature, oxide thickness, ...)
  - Orientation effects
    ($\mu_0$, skewed doping, ...)
- Countermeasures
  - Same variant and orientation
  - Parallel connections instead of larger transistors
  - Spatial proximity
- Common centroid

[Research Source: Hastings: The Art of Analog Layout’01]
Placement Constraints - Symmetry

Differential circuits: symmetrical behavior

Device matching

“Symmetrical” routing requires “symmetrical” placement

[Cohn et al.: Analog Device-Level Layout Automation'94]
State of the Art

• Sensitivity analysis
  – Parasitic devices $\rightarrow$ matching, symmetry
    [Malavasi et al. TCAD’96]
  – Net sensitivities $\rightarrow$ matching [Chen et al. IEE Proc. G’92]
• Graph isomorphism $\rightarrow$ symmetry
  [Kole et al. ISCAS’94] [Hao et al. ICCCS’04]
• Building blocks $\rightarrow$ matching (sizing) [Massier et al. TCAD’08]
• Retargeting using hierarchical symmetry
  [Bhattacharya et al. ASP-DAC’04]
• Circuit hierarchy not considered
  – Possibly missing constraints
  – Infeasible for hierarchical placement
Hierarchical Placement

- Plantage
  [Strasser et al., ICCAD’08]
- Placement generation controlled by inherent hierarchy
- Placement constraints within and among groups
  - Matching
  - Symmetry
  - Proximity
- Similar approach:
  [Lin et al., DAC’08]
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Flow Chart of New Approach

- netlist
- building blocks
- symmetry
Automatic Structure Analysis

- **Structure recognition**
  - Comparison with building blocks from library
  - Resolution of ambiguities
  - [Massier et al. TCAD’08]

- **Symmetry analysis**
  - Propagation of symmetry-pairs starting from differential pair
  - similar to [Arsintescu et al. ICCD’96]
Flow Chart of New Approach

1. netlist
2. building blocks
3. symmetry

- constraint graph (netlist)
- constraint graph (building blocks)
- constraint graph (symmetry)
Constraint Graph (Symmetry)

- Symmetry pair $\rightarrow$ matching constraint (symmetry)
- Symmetry pairs $(d,d')$ of same axis $\rightarrow$ symmetry constraint

$$\forall (d,d') \left( \frac{x_d + x_{d'}}{2} = c \land y_d = y_{d'} \right)$$

- $x_d, x_{d'}$: device coordinates
- $y_d, y_{d'}$: coordinates
- $c$: axis coordinate

Constraint graph (symmetry)
Constraint Graph (Symmetry)

- Symmetry pair → matching constraint (symmetry)
- Symmetry pairs \( (d, d') \) of same axis → symmetry constraint

\[
\forall (d, d') \left( \frac{x_d + x_{d'}}{2} = c \land y_d = y_{d'} \right)
\]

\( x_d, x_{d'} \) device coordinates
\( y_d, y_{d'} \) coordinates
\( c \) axis coordinate

- Elimination of \( c \) → complete graph

constraint graph (symmetry)
Constraint Graph

- constraint graph (building blocks)
- matching constraint
- proximity constraint
- constraint graph (netlist)
- constraint graph
- matching constraint
- symmetry constraint
- constraint graph (symmetry)
Flow Chart

Netlist → Building Blocks → Symmetry

Constraint Graph (Netlist) → Constraint Graph (Building Blocks) → Constraint Graph (Symmetry)

Hierarchical Placement Rules
Conflict Avoidance

• Priority order $T_i$:
  1. Matching constraints (symmetry)
  2. Matching constraints (building blocks)
  3. Proximity constraints (building blocks)
  4. Symmetry constraints
  5. Proximity constraints (netlist)

• Criteria, e.g., differential principle
Hierarchy Generation

- Controlled by priority order $T_1$:
  1. Matching constraints (symmetry)
  2. Matching constraints (building blocks)
  3. Proximity constraints (building blocks)
  4. Symmetry constraints
  5. Proximity constraints (netlist)

- $MG_{S/B}$: Matching group (symmetry / building blocks)
- $SG$: Symmetry group
- $PG_N$: Proximity group (netlist)
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## Hierarchy Generation

<table>
<thead>
<tr>
<th>Circuit</th>
<th>Number of transistors</th>
<th>Groups</th>
<th>Runtime [s]</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Number</td>
<td>Size</td>
</tr>
<tr>
<td>Miller$^1$</td>
<td>9</td>
<td>5</td>
<td>2 – 4 (Ø 2,6)</td>
</tr>
<tr>
<td>Example</td>
<td>10</td>
<td>8</td>
<td>2 – 4 (Ø 2,5)</td>
</tr>
<tr>
<td>Fully Differential OTA$^2$</td>
<td>30</td>
<td>19</td>
<td>2 – 5 (Ø 2,5)</td>
</tr>
<tr>
<td>Folded Cascode OTA$^1$</td>
<td>22</td>
<td>17</td>
<td>2 – 3 (Ø 2,2)</td>
</tr>
<tr>
<td>Buffer$^3$</td>
<td>42</td>
<td>21</td>
<td>2 – 14 (Ø 2,9)</td>
</tr>
</tbody>
</table>

- Runtime of placer ~ group size

$^1$ [Laker, Sansen: Design of Analog Integrated Circuits 94]
$^2$ [Galdi et al. JSSC’08],  $^3$ [Fisher et al. JSSC’ 87]
Comparison with Cadence Virtuoso

Number of Constraints

Constraints
- cluster (hierarchical)
- symmetry (pairs)
- cluster (devices)
- same variant
- alignment

I: Cadence Virtuoso Schematic Editor XL; N: New approach

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Experimental Set-up

- sized schematic of fully differential ota
- hierarchical placement using *Plantage* [Strasser et al.; ICCAD’08]
- automatic routing (Cadence Chip Assembly Router)
- parasitics extraction (Cadence Assura)
- post layout simulation (Cadence Spectre)
- new approach

industrial tool: Circuit Prospector of Cadence Virtuoso Schematic Editor

unconstrained
Schematic of Fully Differential OTA

[Galdi & al., JSSC’08]
Hierarchical Placement Rules of FD OTA

MG_{S/B}: Matching group (symmetry / building blocks); SG: Symmetry group;
PG_{B/N}: Proximity group (building blocks / netlist)
Layout and Post Layout Simulation

<table>
<thead>
<tr>
<th>performance</th>
<th>unconstrained</th>
<th>industrial</th>
<th>new approach</th>
</tr>
</thead>
<tbody>
<tr>
<td>$A_0$ [dB]</td>
<td>72</td>
<td>72</td>
<td>72</td>
</tr>
<tr>
<td>$f_0$ [MHz]</td>
<td>22</td>
<td>22</td>
<td>22</td>
</tr>
<tr>
<td>$V_{offset}$ [$\mu$V]</td>
<td>140</td>
<td>93</td>
<td>-6.6</td>
</tr>
<tr>
<td>CMRR [dB]</td>
<td>78</td>
<td>76</td>
<td>110</td>
</tr>
</tbody>
</table>

Post layout simulation

differential pair

current mirrors
Conclusion

• Generation of hierarchical placement rules
  – Structure and symmetry analysis
  – Assignment of constraints to constraint graph
  – Generation of hierarchical groups
  – Constraints within and among groups: matching, symmetry, proximity

• Experimental results
  – Feasible for hierarchical placement approaches
  – Comprehensive constraint generation
  – Improved post layout performance

Thank you!
Constraint Assignment (Netlist)

• Connections → proximity constraints (netlist)
• Beneficial for routing

Nodes = Devices

Edges = Constraint Requirements
Here: Proximity Constraint (Netlist)

Constraint Requirement Graph (Netlist)
Constraint Assignment (Building Blocks)

- Two transistor blocks → matching constraints (building blocks)
- Larger blocks: additional proximity constraint (building block)
Conflict Avoidance

Priority order $T_1$:

1. Matching constr. (symmetry)
2. Matching constr. (building b.)
3. Proximity constr. (building b.)
4. Symmetry constr.
5. Proximity constr. (netlist)

Criteria:

- Differential principle
- Increasing size
Generated Placement

Placement Constraints:
- alignment
- common centroid
- symmetry axis
- group

- current mirrors
- differential pair
Hierarchically Bounded Enumeration

Enumeration of placements of fundamental module sets
Enhanced Shape Functions

- Hierarchical approach
- Good for semi-automatic layout generation
- High flexibility
- Enhanced shape function for each node of hierarchy
- Close proximity of modules is achieved by hierarchy

Enhanced Shape Addition