“Thinking outside of the chip”

Using co-design to optimize interconnect between IC, Package and PCB

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Current “Over-the-wall” design process

IC Layout                                Package design                                       PCB layout

Higher Cost
Custom package & Increased layers on PCB
Longer Development Cycles
Increased complexity for PCB and Package
Co-Design: A parallel design process

IC Layout → Package design → PCB layout

Reduced design cycles
Less expensive, standard package
Fewer PCB layers (lower cost)
Co-Design: What’s driving it...

- SOC total pin counts surpassing 30,000
  - IO pad-ring generation no longer a simple task.
    - Staggered, multi-row placement
    - Area IO placement
  - Flip-chip development
    - Managing, placing and optimizing bumps
    - RDL routing
- High Speed serial I/Os
  - I/O buffer scaling for minimum power
  - Interconnect modeling across package and PCB
  - Power delivery across PCB, Package and IC
  - Trade off analysis between wire bond and flip-chip
  - More accurate 3D (full-wave) analysis for package and PCB interconnect structures
- Package costs killing profit margin
  - Drive to standard packages
    - Package selection no longer an afterthought
- PCB layout is a bottle-neck to volume
  - Interconnect/Routing problems on the PCB are amplified by the high pin count devices.
  - Additional layers driving up cost
IC, Package and PCB physical interfaces

IC
- I/O Buffers
- Core Blocks
- RDL Routing
- Flip-chip bumps

Package
- Off-Chip Passives
- Package Pins (Balls)
- Die abstract

PCB
- PCB footprint (could include breakout)
What exactly needs to be optimized?

**IC level**
- I/Os
  - Peripheral (including multi-row stagger)
  - Area (including direct bumping)
- Bumps (C4s)
- Interposer

**Package level**
- Bumps (C4s)
- Bond fingers
- Package pins
- Interposers

**PCB level**
- Package pins (including breakouts)
Where does co-design fit in the flow...
Co-Design: Some of the challenges...

- Design teams often not in same location
  - Package and/or PCB layout outsourced
- EDA tools don’t often play well together
  - No tool exists today that easily bridges the gap
  - Part time users, must be easy to use
- Requires cross design domain knowledge
  - Engineers must be willing to expand their knowledge
  - It’s no longer clear where the handoff is between tools
Cross domain tasks and data sharing

What format is used for data exchange?
Which design tool and team is responsible for what...

Constraints, Connectivity, Physical placement

**IC place & route**
- Placement
- Connectivity assignment
- Constraint assignment
- RDL routing

**Package design**
- Package symbol
- Bump array generation
- Connectivity optimization
- Constraint assignment
- PCB level footprint
- Pin delays
- Accurate package model

**Board design**
- Placement
- Break-out routing
- Constraint assignment
- RDL routing

Excel LEF/DEF GDSII Gerber OpenAccess
3D packaging, Now what...

- 3D packaging will require optimizing in the Z direction.
  - SiP (Stacked die), PoP, 3D IC (TSV interconnect)
  - Interposer planning and optimization
  - Optimization from chip to chip to package to package to PCB
    - Multiple technologies integrated together
What are designers doing now?

- MS Excel driven flows
  - Unaware of physical data
  - No routability assessment
  - No DRC checking
  - No asymmetrical placement
  - IO’s, Bumps
- Static data
- No constraint management
- Limited connectivity management
What are designers doing now?

- PCB design groups are generating ball pin maps (ballout)
  - Breakout to breakout strategy
  - Typically stops at the package pin
  - What about the chip inside the package?
  - What about the routability of the package substrate?
  - Limited knowledge of any swap rules or constraints
  - No connectivity management between design domains
    - Automatic Pin mapping (signal name changes)
- FPGA pin optimization is a reality
  - PCB driven, FPGA pin assignment design tools exist today
  - Automates PCB and schematic symbol generation
  - Relies on up-to-date models from the FPGA vendors
    - Correct-by-construction pin assignments
What are designers doing now?

- Power delivery and signal integrity
  - Power Delivery Network from PCB through Package onto Chip
  - Can be used to optimize bypass capacitor placement on PCB/Package
  - Methods to link multiple databases together for interconnect modeling
  - Package interconnect no longer ignored
  - More complex EM modeling requirements
    - 2D vs. 3D, Quasi-static vs. Full-Wave, etc.
Where we need to go from here...

- Tighter integration between design groups and tools
  - System level Connectivity & Constraint management
    - Signal mapping between design domains
  - Rule based assignment and optimization
    - Library of standard bus’s
      - Computer, Storage, Peripheral
  - True bi-directional data exchange
    - Shared data model between tools
    - ECO from any domain
    - More robust die abstract models
      - RDL routing, Power routing, Blocks, etc.
- System level PDN and SI analysis to drive I/O buffer design
  - Lowest power I/O settings
  - Standard model connection protocol
Co-Design Optimization Flow...

Connectivity & Constraint capture
Signal mapping between IC, Package and PCB

Physical based unraveling (optimizing) environment

- I/O to Core Optimization
- Die Attach to I/O Optimization
- Package to Die Attach Optimization (Bond Finger or Bump)
- PCB to Package Optimization

Physical Instances/Abstracts
Swap Rules
Bus Standards/User Defined

IC floorplan
Package Pin-out
PCB Placement
Co-Design: Board level optimization...

Before optimization

After optimization
PCB level Routing results...

No Optimization

With Optimization

26% Cost Reduction

Courtesy of:
Thank you for your attention.