Via Pillar-aware Detailed Placement

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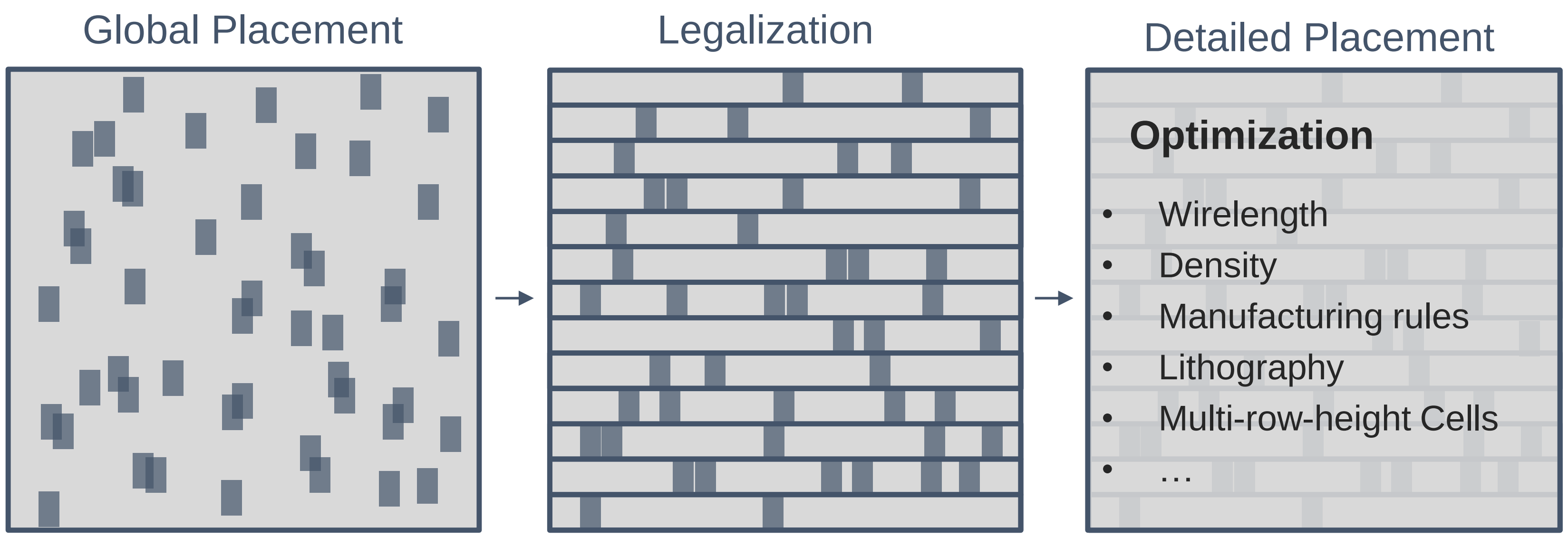
Outline

- Introduction
- Algorithm
- Experiment Results
- Conclusion

INTRODUCTION

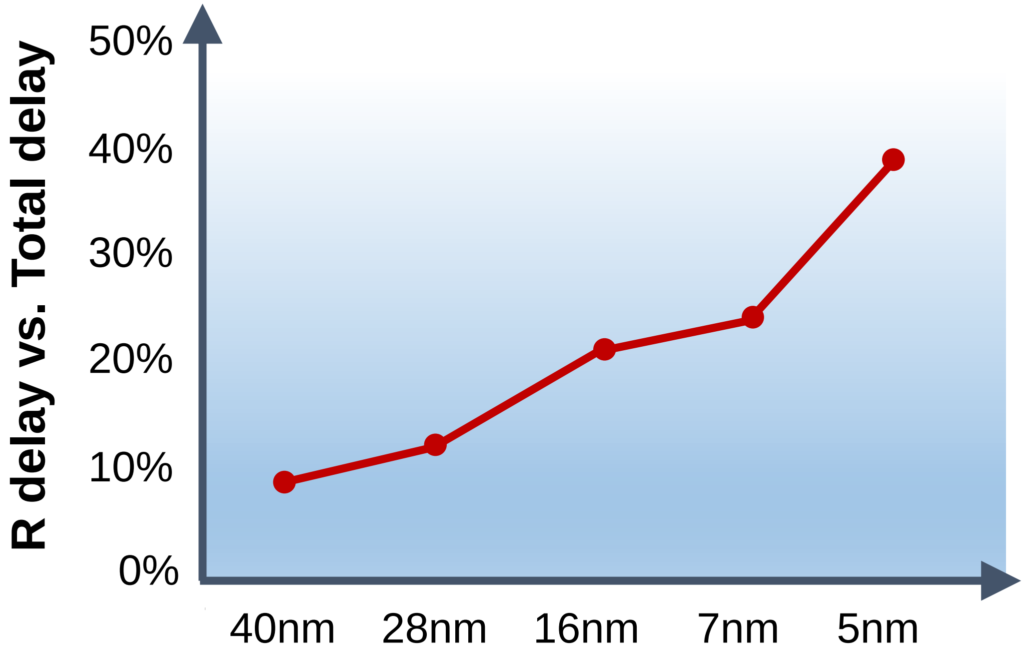
Detailed Placement

- In the VLSI physical design flow, placement consists of 3 stages:
  - (1) Global placement
  - (2) Legalization
  - (3) Detailed placement
- Detailed placement focuses on improving the legalized placement solution, while keeping its legality



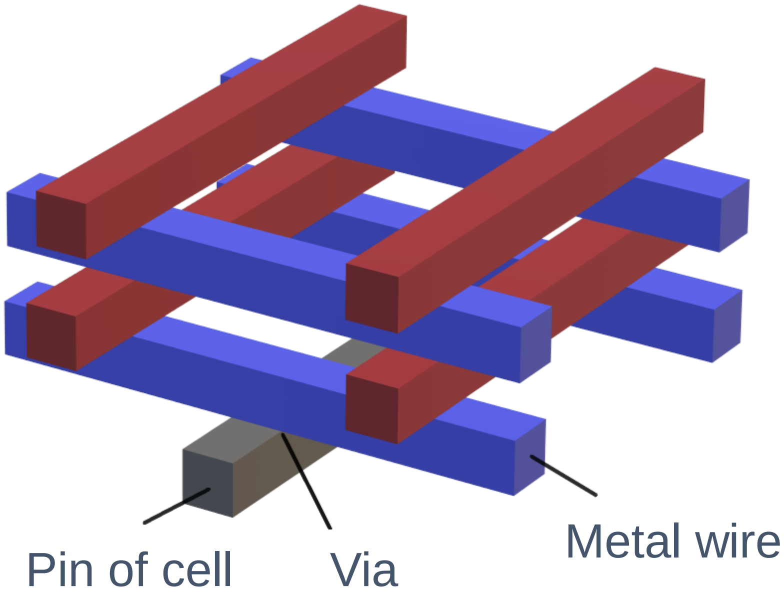
Via Pillar

- Feature size has shrunk down to 7 nm and beyond
  - The impact of wire resistance is significantly growing
  - The circuit delay incurred by the metal wires is noticeable raising
- A new technique “Via Pillar” (or via pillar) is proposed



L. -C. Lu, Physical Design Challenges and Innovations to Meet Power, Speed, and Area Scaling Trend", ISPD, 2017

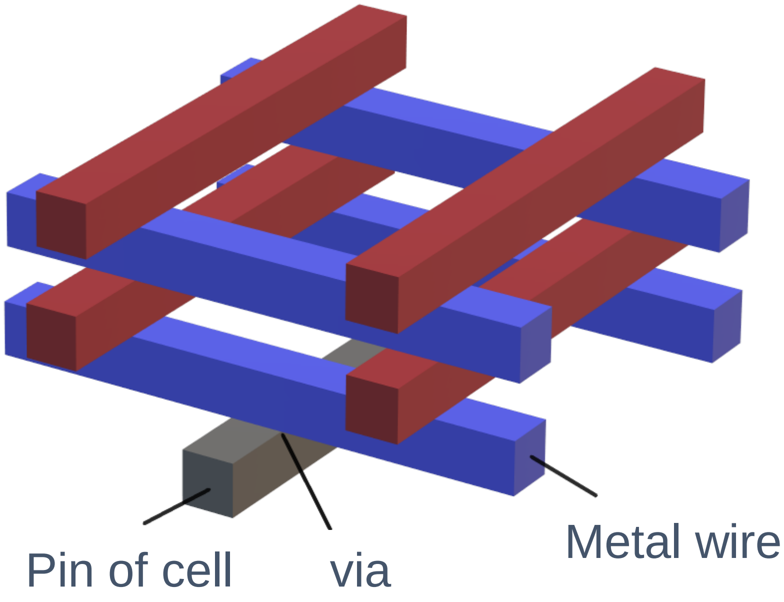
Structure of Via Pillar



Structure of Via Pillar

- Multiple vias
- Multiple metal wires
- Cross multiple layers (generally)

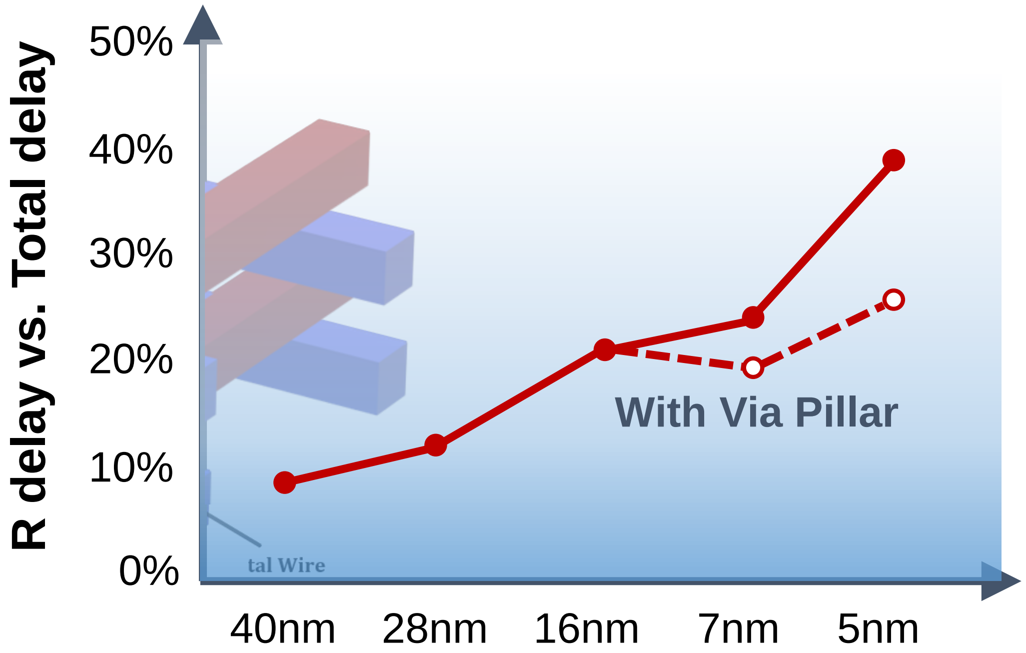
Benefits of Via Pillar



Benefits of Via Pillar

- Reduce Wire Resistance
- Reduce Circuit Latency
- Enhance Reliability
- Enhance EM robustness

Benefits of Via Pillar



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Problem on Via Pillar Insertion

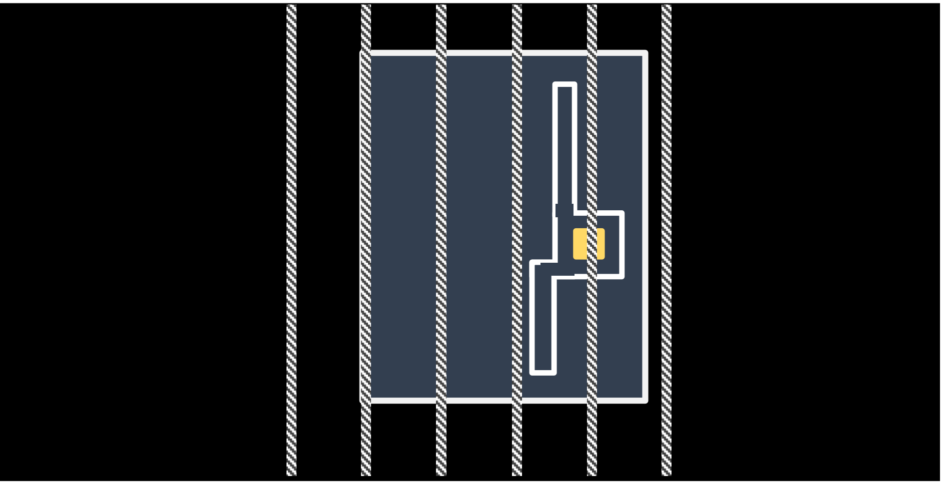
Major issues that cause poor Insertion success rate:

- Track Alignment Issue
- Power/Ground Stripe Overlapping
- Insufficient Margin Area

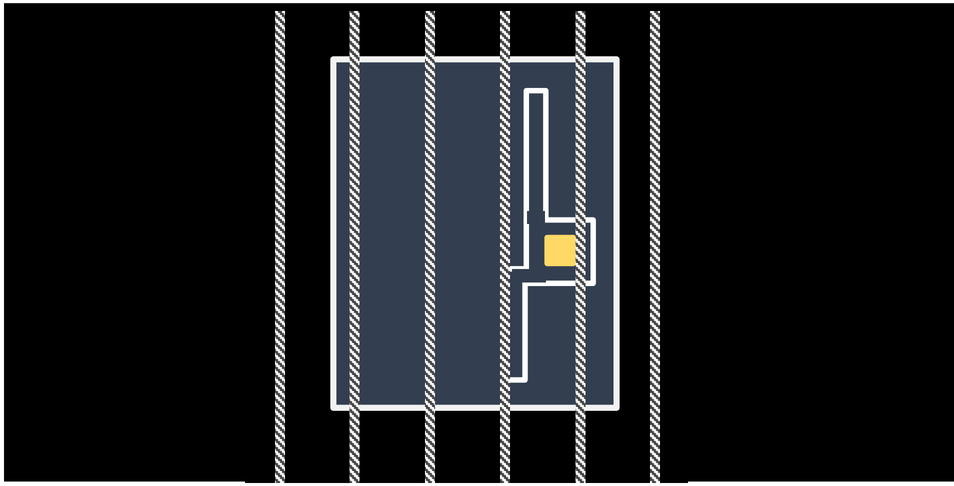
Track Alignment Issue

- In our experiments, we found that the via pillar insertion may fail when the access point is not at a certain position w.r.t. its adjacent tracks

M4 (success)



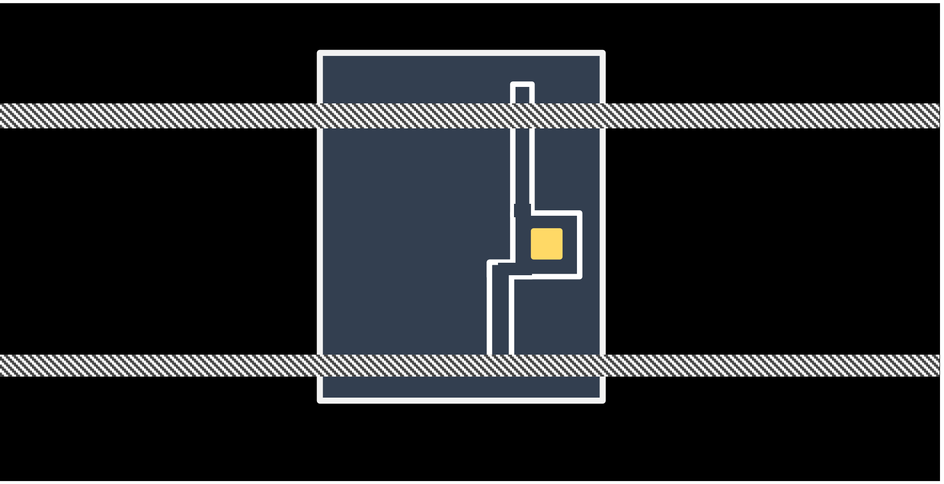
M4 (failure)



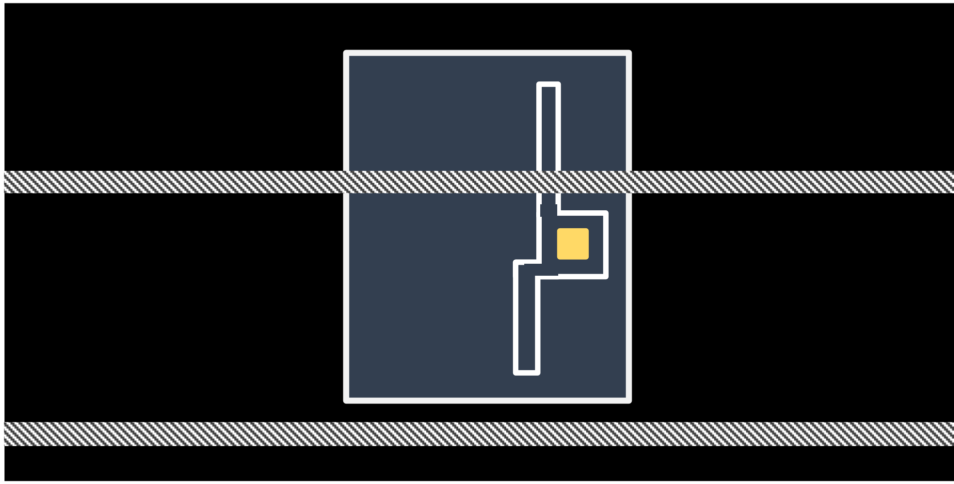
Track Alignment Issue (cont'd)

- In our experiments, we found that the via pillar insertion may fail when the access point is not at a certain position w.r.t. its adjacent tracks

M5 (success)

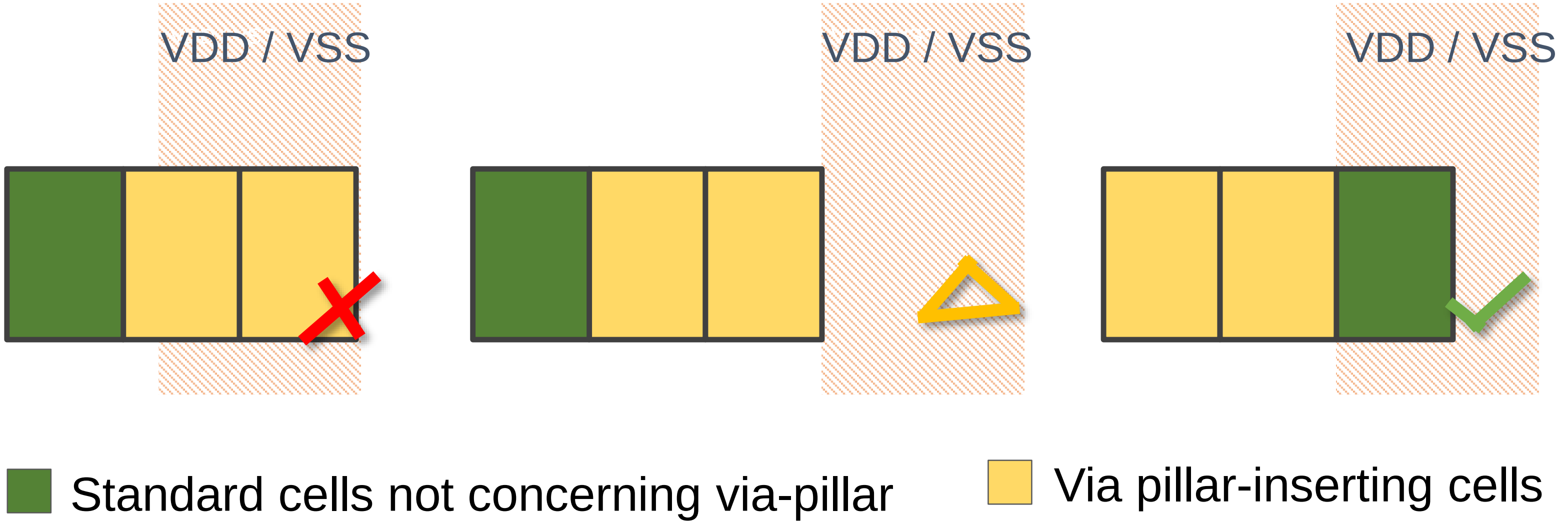


M5 (failure)



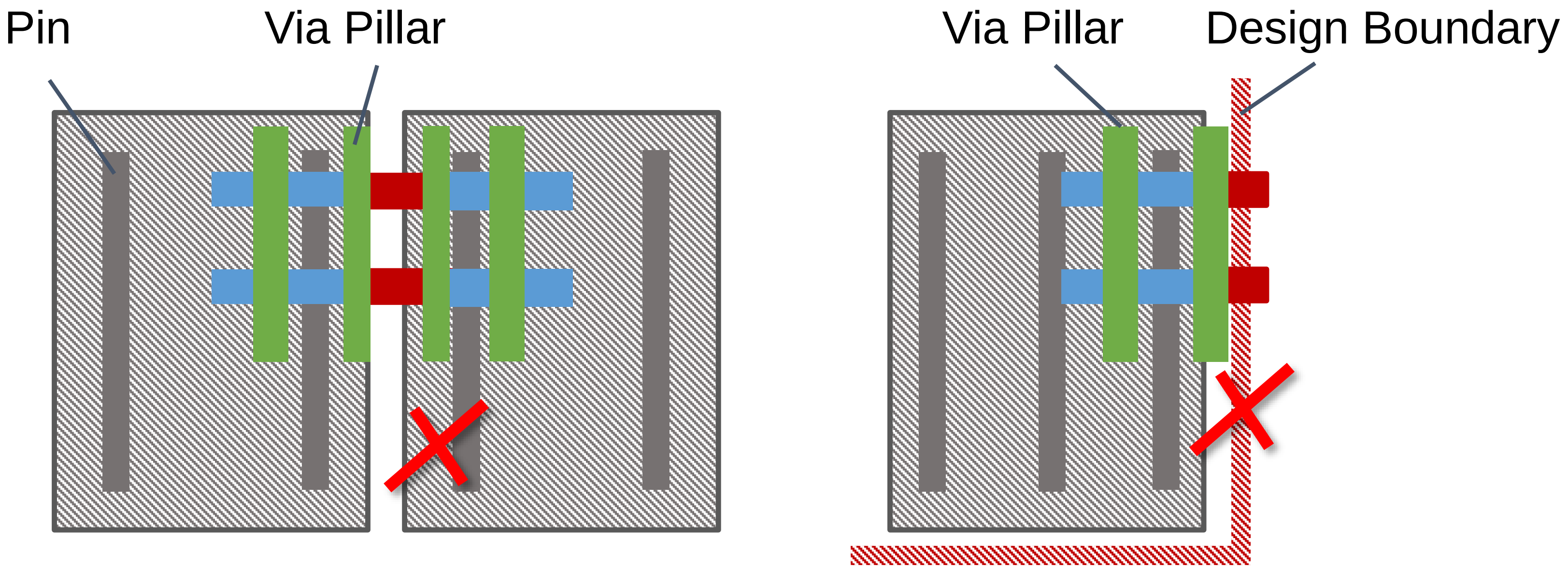
Power/Ground Stripe Overlapping

- If the structure overlaps with a power/ground (PG) stripe, the insertion of the via pillar will fail
- Denser or wider PG strips will result in fewer eligible positions, more difficult to optimize the result



Insufficient Margin Area

- If a via pillar structure overlaps with another via pillar or design boundaries, the insertion will fail



Previous Works

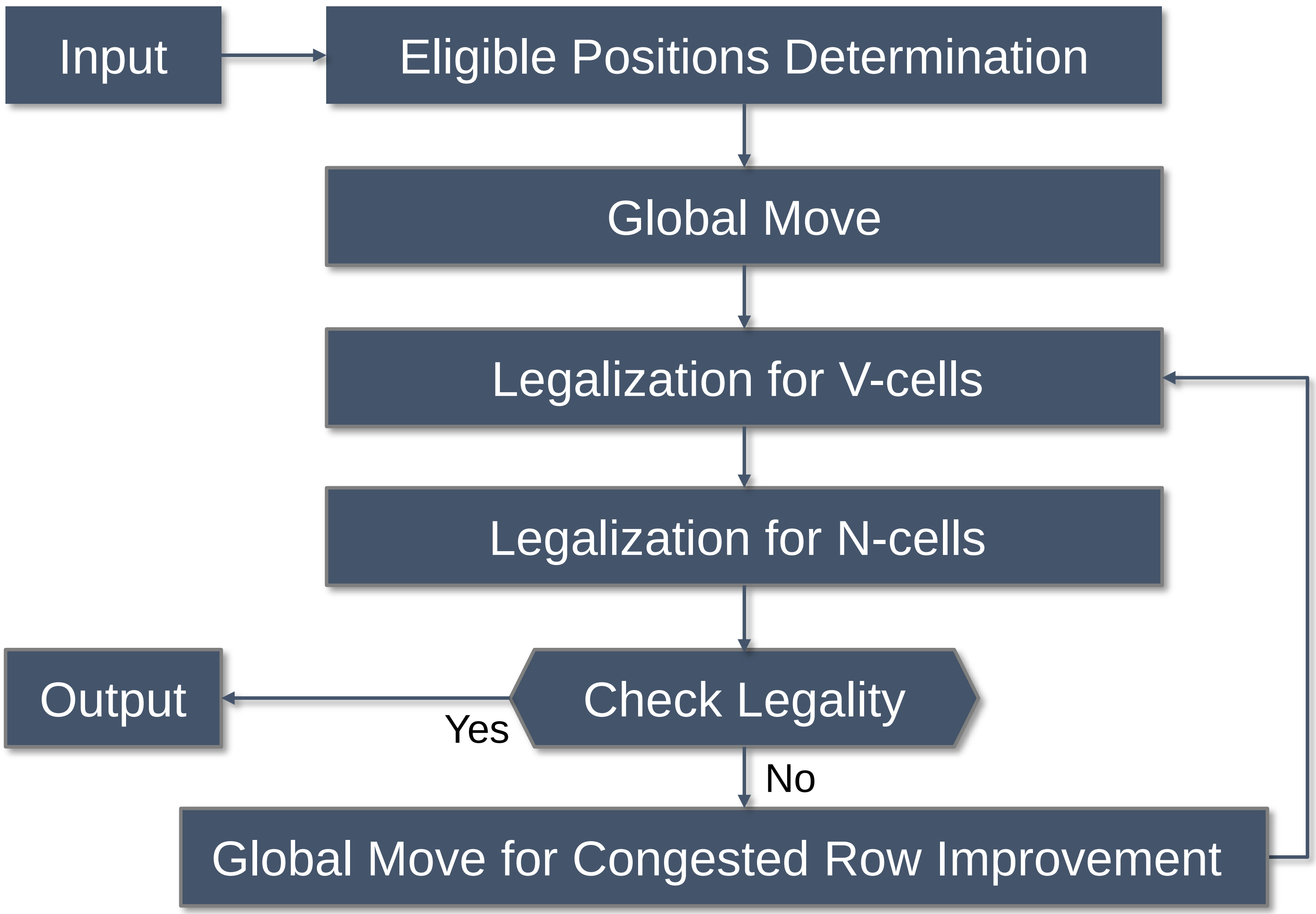
- The research on detailed placement have been developed in decade that address various issues
  - Wirelength
  - Density
  - Manufacturing rules
  - Lithography
  - Multi-row-height Cells
- However, none of these works has focused on via pillar insertion in the detailed placement stage

ALGORITHM

Terminology

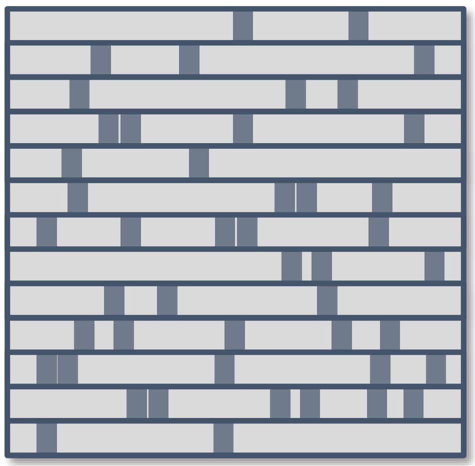
- An N-cell is a cell that is not concerning via pillar (normal cell)
- A V-cell is a cell that will be inserted a via pillar
- An eligible row/site/position indicates the position with maximized insertion rate
  - No track alignment issue
  - No overlap with any PG stripe
- MDC is the maximum displacement constraint that prevents from a large movement

Algorithm Flow

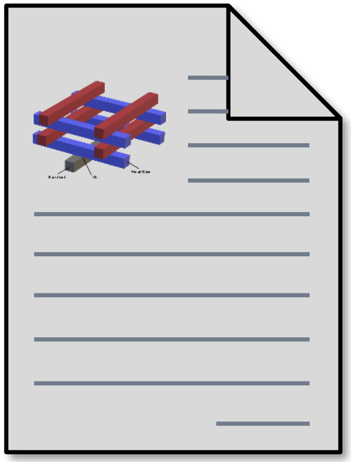


Input

- Placement Result



- Configure file



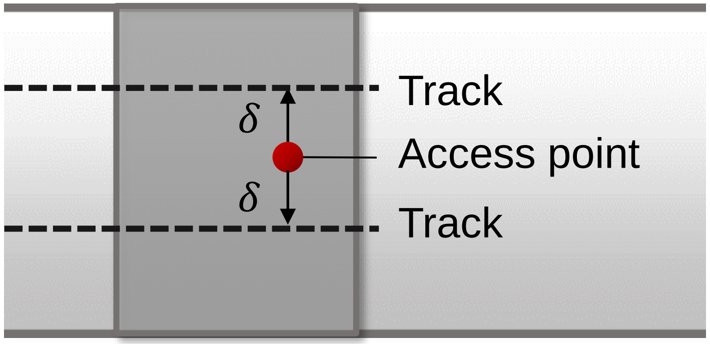
List of via-pillar inserting cells

Eligible Positions Determination

- To enhance the via pillar insertability, we determine all the eligible positions for all V-cells

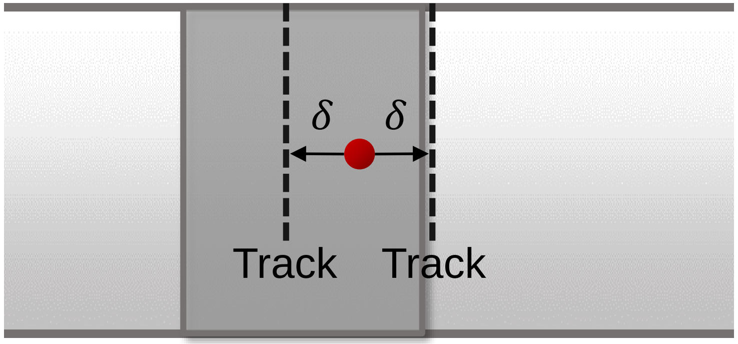
1. Filter out positions overlap with PG stripe
2. Filter out positions with track alignment issue

Eligible Row



For each horizontal layers

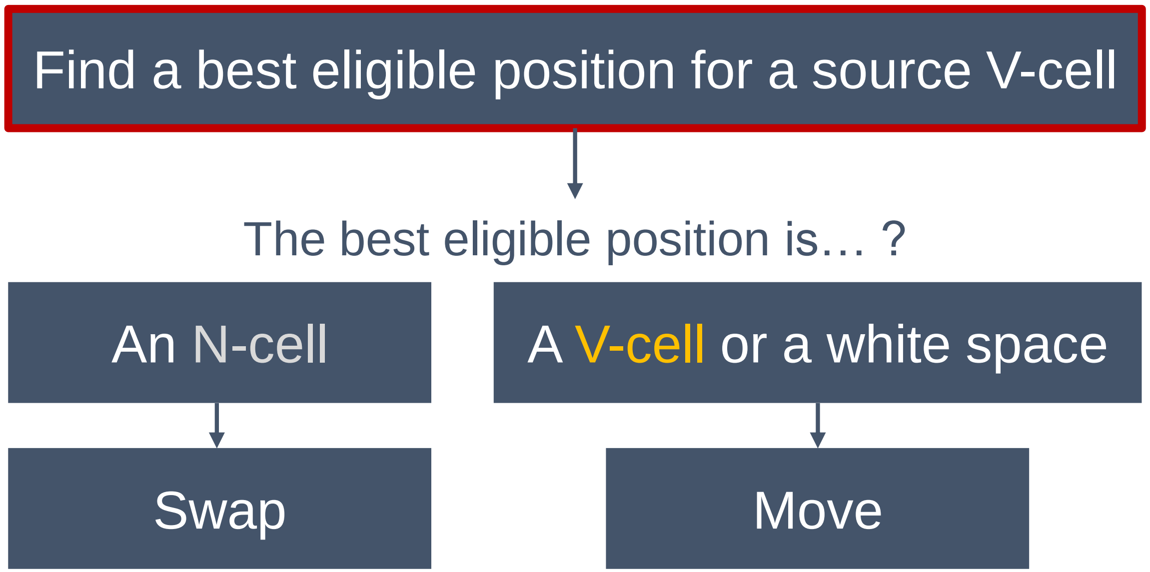
Eligible Site



For each vertical layers

Global Move

- The goal of this step is to move all V-cells in ineligible rows to eligible sites



Global Move (cont'd)

- For each V-cell, We first find a best eligible position
- We traverse all eligible sites within MDC and evaluate them by the cost function

$$cost = \alpha \cdot \Delta W + \beta \cdot D + \rho P_C + \sigma(1 - P_S)$$

$$P_C = \frac{Area(Ncells)}{Area(Row)} \cdot \Delta Area(cell)$$

$$P_S = \frac{\#eligible\ sites}{\#total\ sites\ in\ row}$$

ΔW: Wirelength improvement (or degradation)

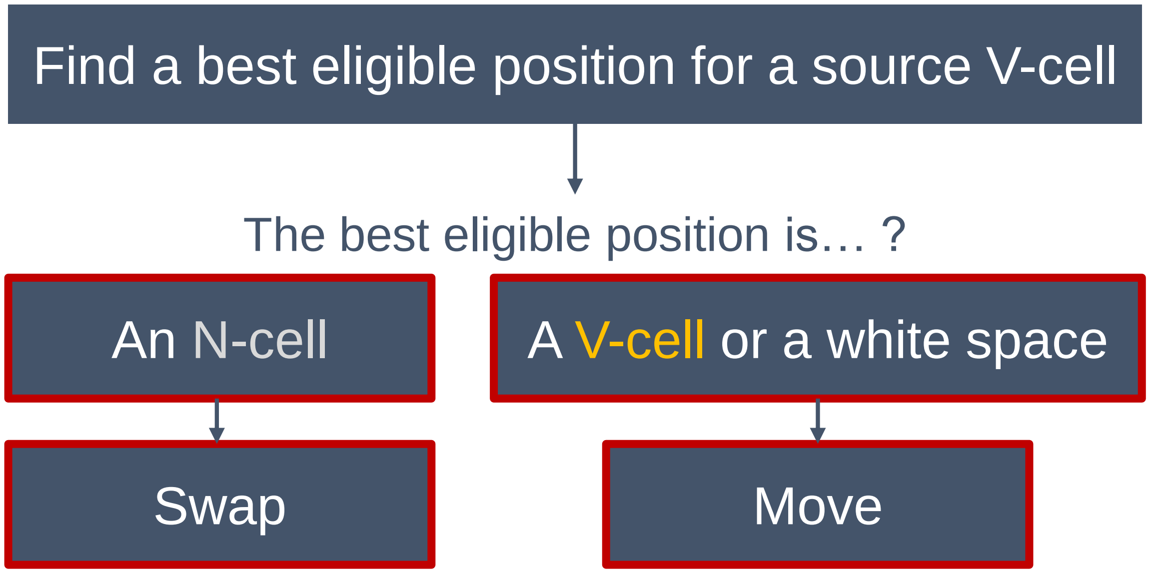
D: Displacement

P_C: Penalty of congested situation

P_S: Penalty of density of eligible sites

Global Move (cont'd)

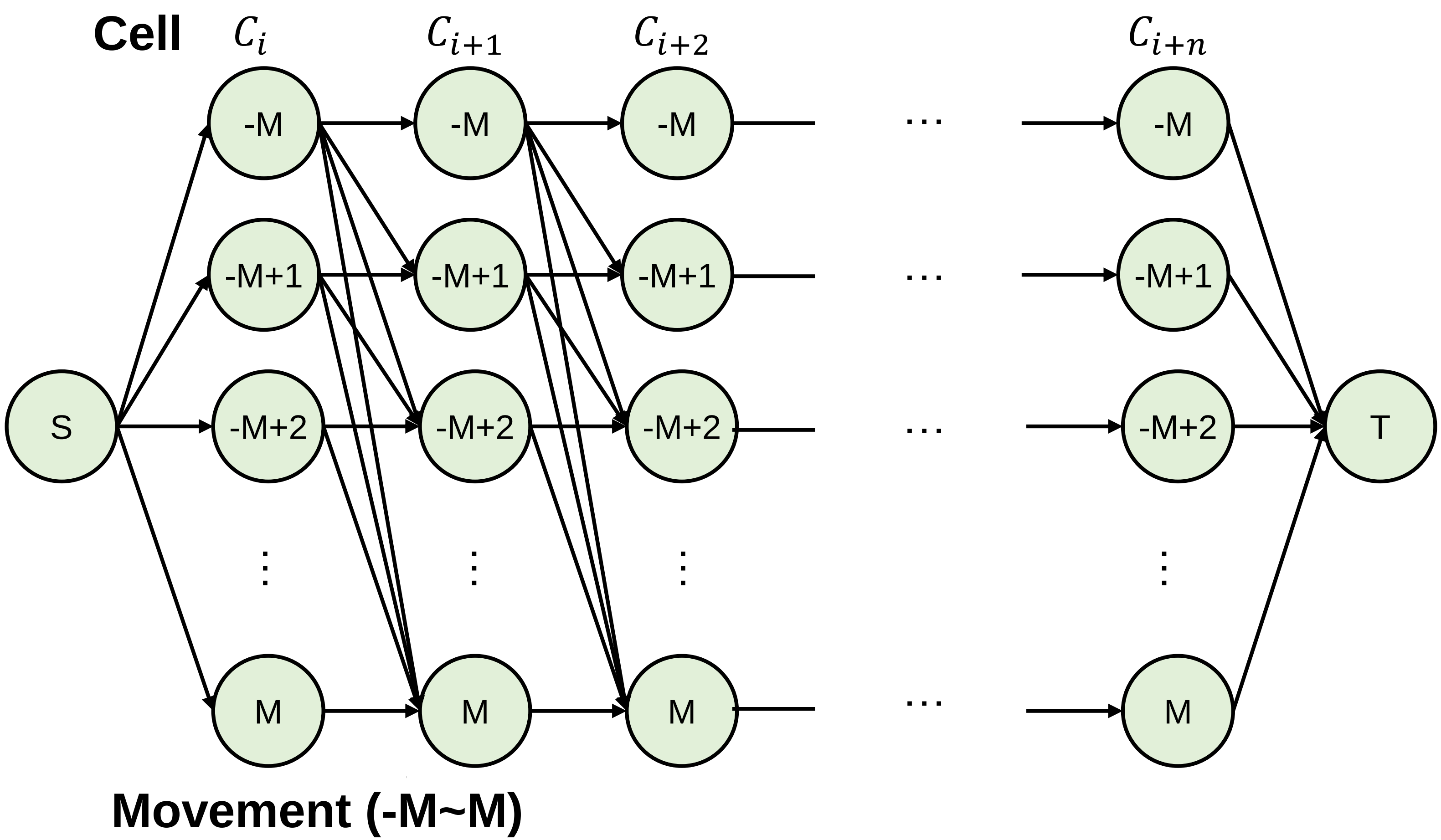
- The overlaps among cells are permitted in this step
- To prevent from the sequence issue, we move a cell to a site if it is occupied by another V-cell



- There should be no V-cell in an ineligible row after this step

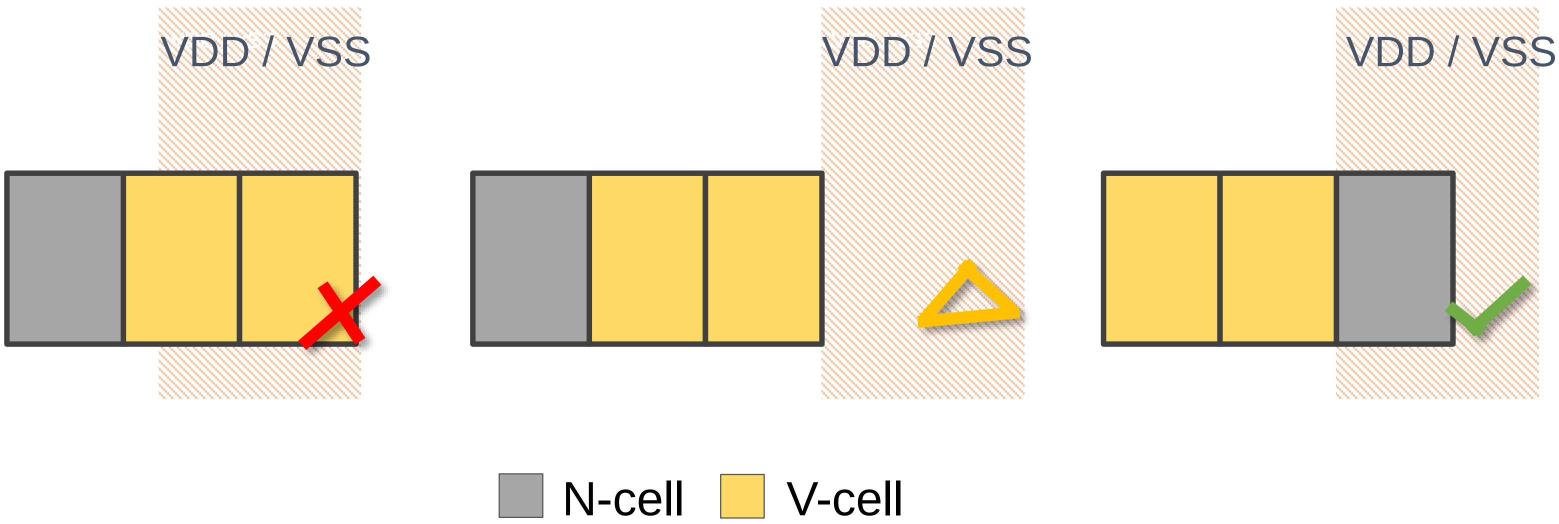
DP-based Legalization Method (cont'd)

- Our legalizer is based on dynamic programming-based detailed placement algorithm [Taghavi et al., ICCAD, 2010]



DP-based Legalization Method (cont'd)

- However, the order of cells among V-cells and N-cells may have to be changed to obtain a result in better quality if the PG stripes are dense or the row is congested



DP-based Legalization Method (cont'd)

- Hence, we divide legalization procedure into two-stage to achieve the effect of re-ordering

Legalization for V-cells

- Resolve overlaps among V-cells
- Ignore the existence of N-cells

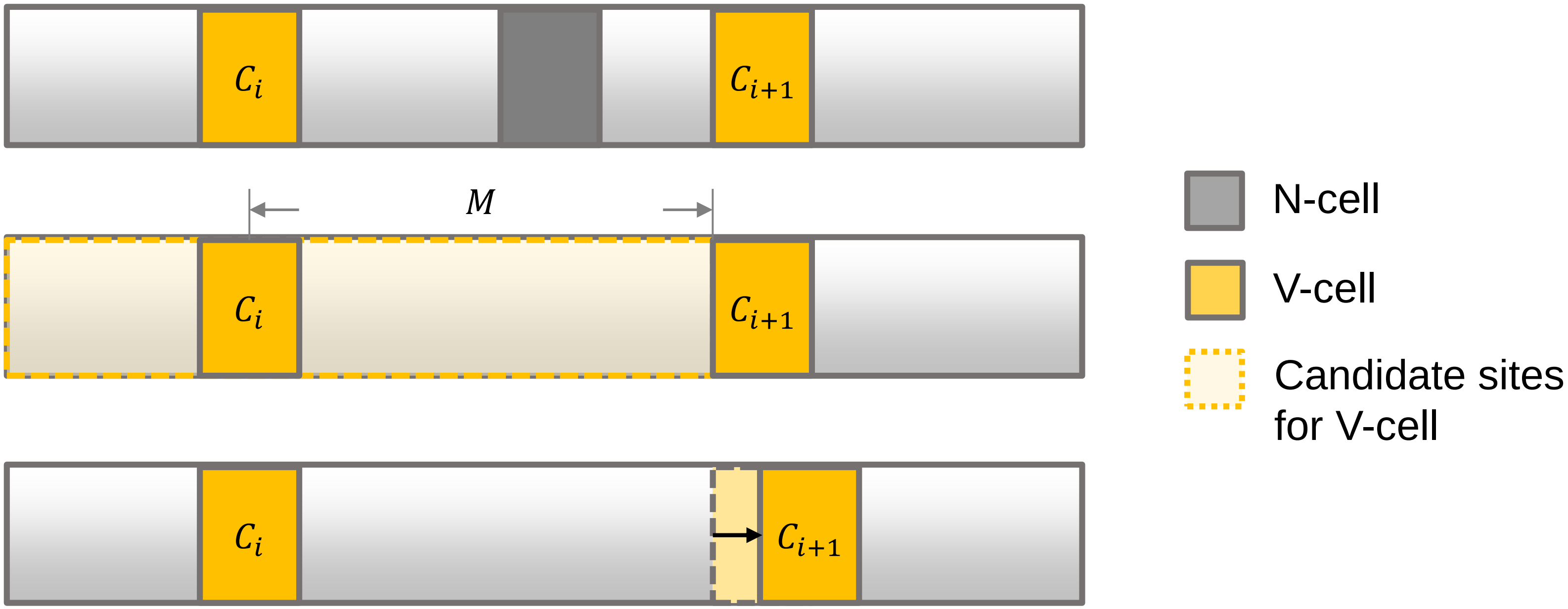
↓

Legalization for N-cells

- Regard the V-cells as obstacles
- Achieve the effect of re-ordering among V-cells and N-cells

Legalization for V-cell

- In the legalization of V-cells, we ignore the existence of N-cells and only legalize for V-cells



Legalization for V-cell (cont'd)

$$cost = \alpha \cdot \Delta W + \beta \cdot D + P_{\mathrm{M}} + P_{\mathrm{E}}$$

ΔW: Wirelength improvement (or degradation)

D: Displacement

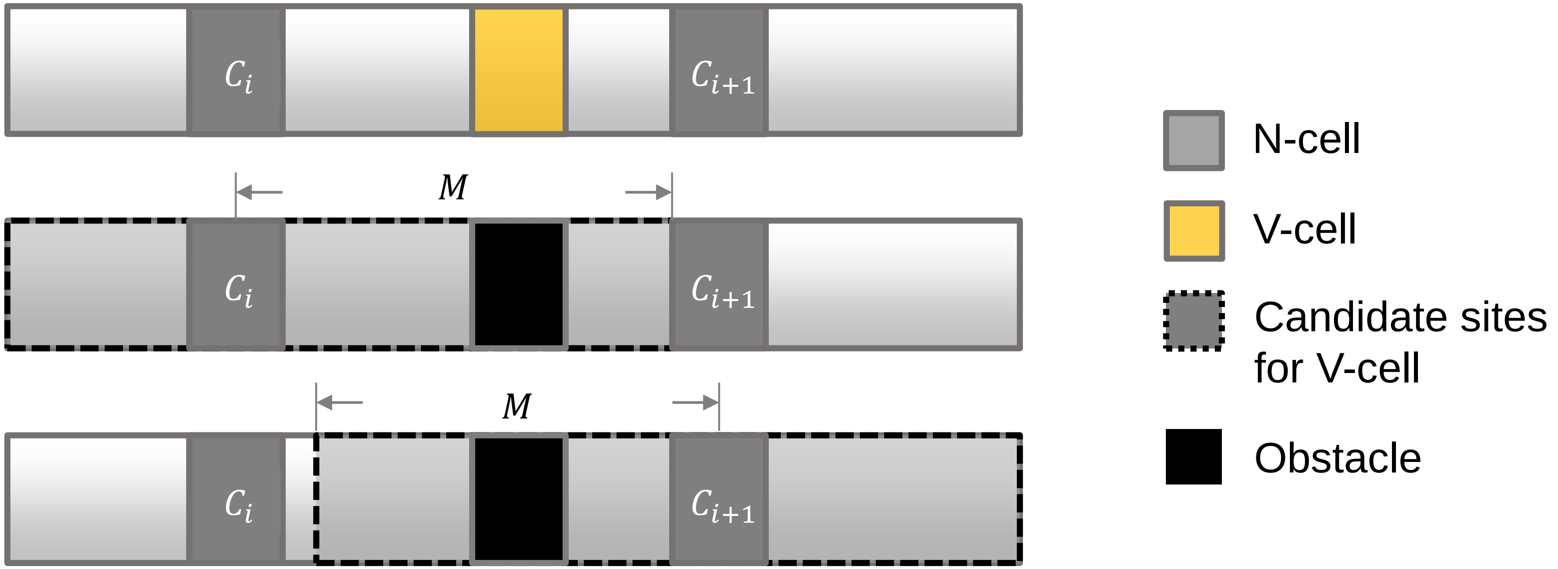
P_M: Penalty for violation of MDC

P_E: Penalty of eligible site alignment

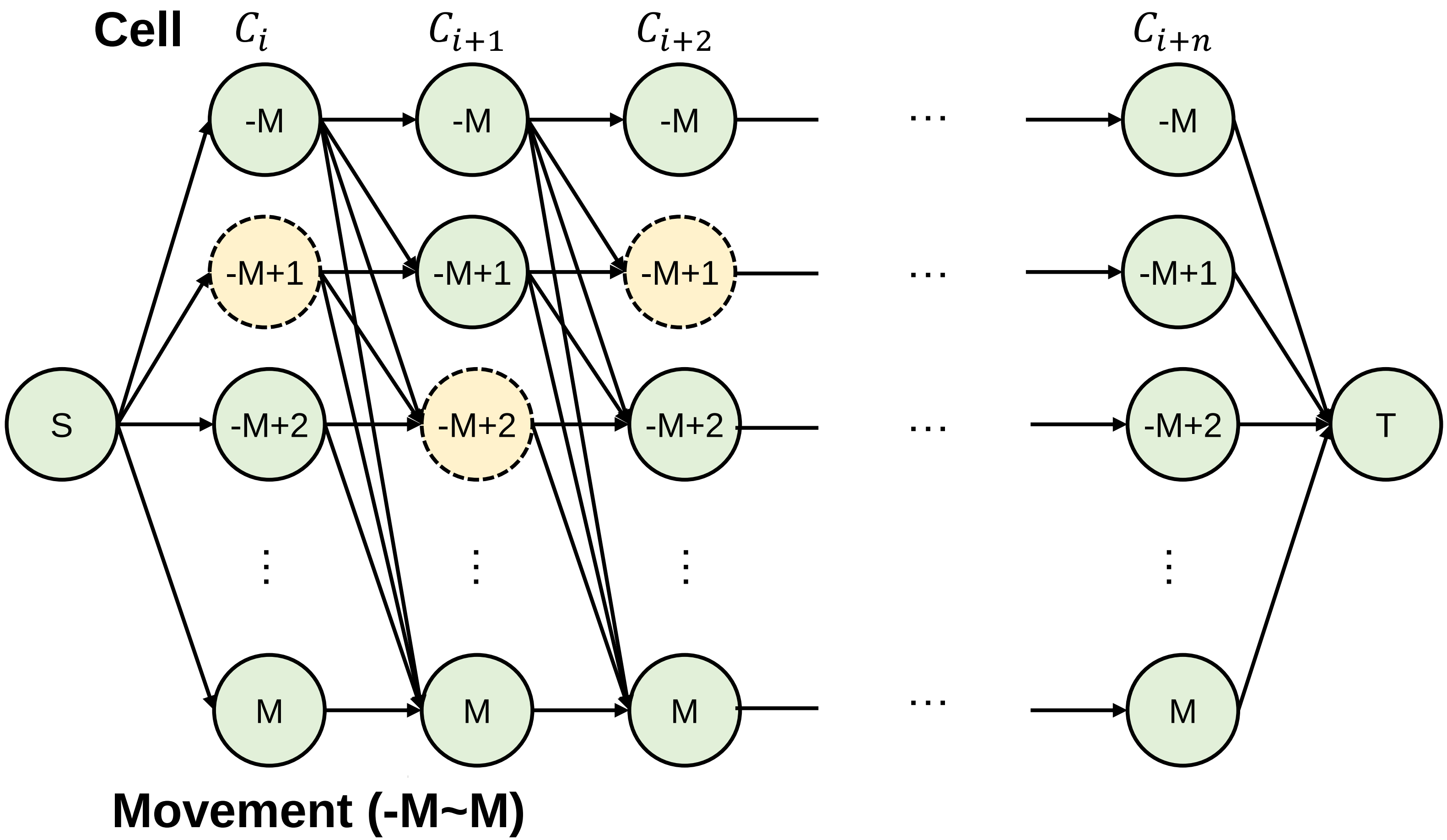
$$P_M = \begin{cases} 0, & diplacement\ \ within\ MDC \\ \infty, & displacment\ beyond\ MDC \end{cases} \qquad P_E = \begin{cases} 0, & if\ the\ site\ is\ eligible, \\ \infty, & otherwise. \end{cases}$$

Legalization for N-cell

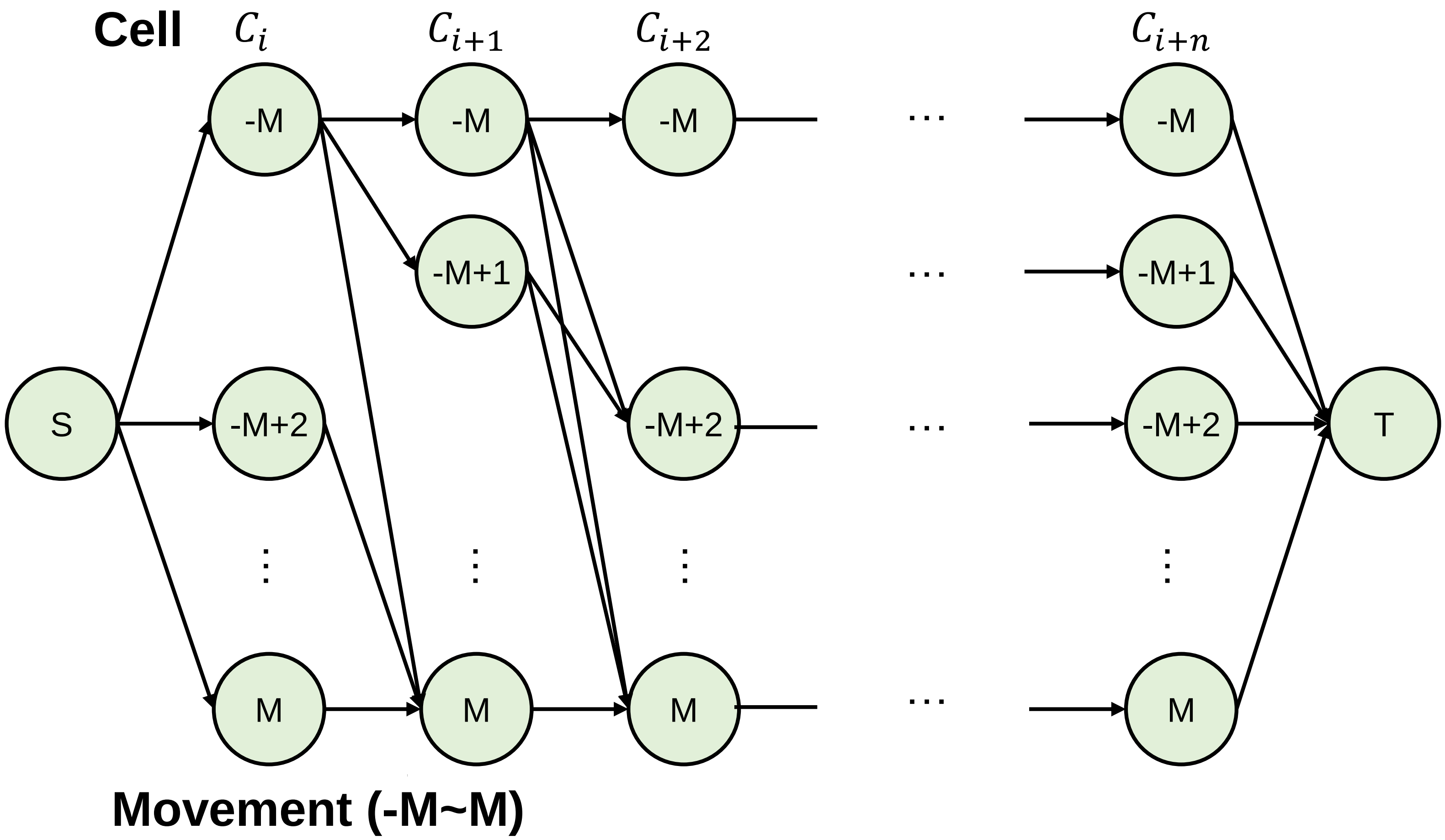
- To achieve the effect of re-ordering among V-cells and N-cells, we regard the V-cells as obstacles without actually place it.



Legalization for N-cell (cont'd)



Legalization for N-cell (cont'd)



Legalization for N-cell (cont'd)

$$cost = \alpha \cdot \Delta W + \beta \cdot D + P_{\mathrm{M}}$$

ΔW: Wirelength improvement (or degradation)

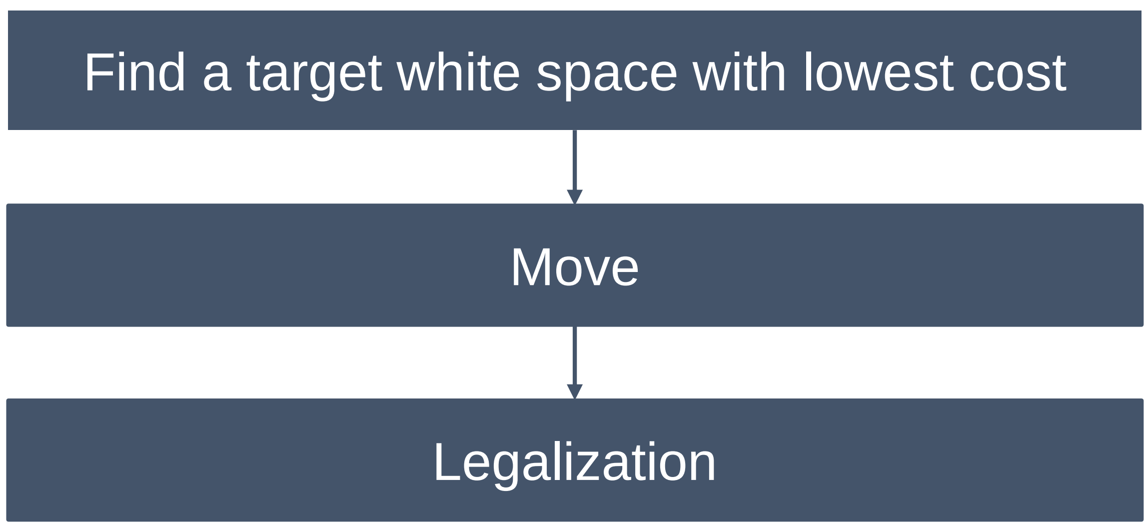
D: Displacement

P_M: Penalty of MDC

$$P_M = \begin{cases} 0, & diplacement\ \ within\ MDC \\ \infty, & displacment\ beyond\ MDC \end{cases}$$

Global Move For Congested Row Improvement

- After legalization, some of the rows are still remaining illegal when cells are highly congested in the rows
- We try to move the cells in a congested row to white spaces with a smallest cost within MDC



Global Move For Congested Row Improvement

$$cost = \alpha \cdot \Delta W + \beta \cdot D + \varepsilon P_V$$

ΔW: Wirelength improvement (or degradation)

D: Displacement

P_V: Penalty of local overlap

$$P_V = overlap\ area\ with\ adjacent\ cells$$

EXPERIMENTAL RESULTS

Environment Setting

- C++ programming language
- The results were generated on a 2.10 GHz Intel Xeon CPU E5-2620 Linux machine with 32GB memories
- Parallel processing in the eligible position determination by 24 threads
- Adopt commercial APR tool "*IC Compiler 2*" to perform via pillar insertion process

Benchmarks

- We integrate the real industrial 16 nm standard cell library into ISPD 2015 placement contest
- Only big-macro-free testcases were adopted
- We create a via-pillar structure which crosses from M1 to M5, with 1, 2, 2, 2 bars and 1, 1, 2, 2 cuts in M2, M3, M4, M5, respectively
- We manually lay PG stripes in each testcase

Characteristics of Benchmark Suit

Design	Cell Area (mm^2)	#Cells	#Nets
mgc_fft_1	0.0584	32281	33307
mgc_fft_2	0.0584	32281	33307
mgc_des_perf_1	0.1790	112644	112878
mgc_matrix_mult_1	0.2427	155325	158527

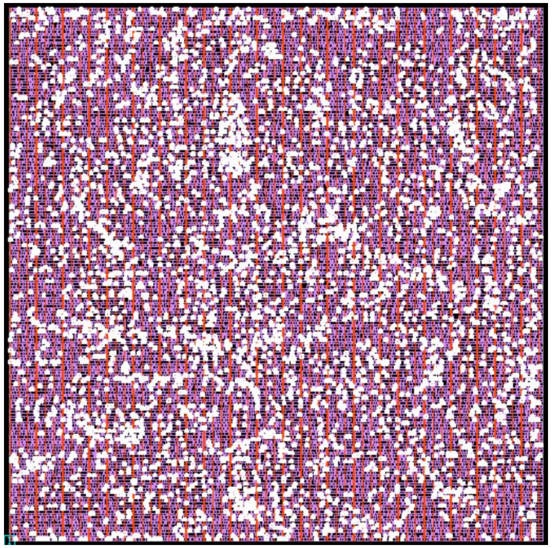
Result on Testcases with PG Stripe

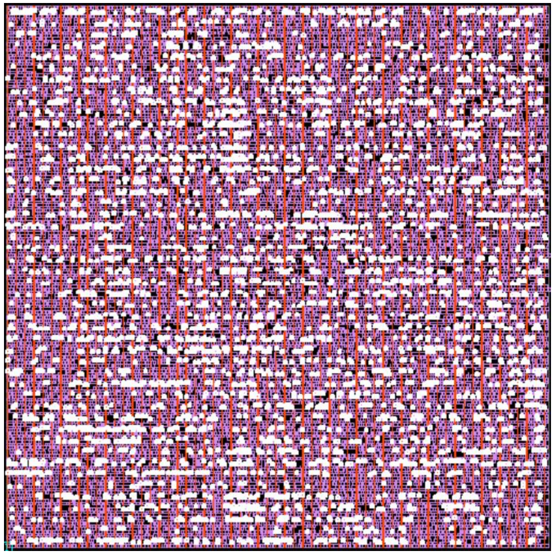
- With PG Stripe & track alignment issue

	fft_1	**fft_2**	**des_perf_1**	**matrix_mult_1**	Average
#Row	192	192	348	383	
#Eligible row	96	96	174	192	
#Cell	32281	32281	112644	155325	
#V-cell	3850	3832	955	13103	
Insertion rate % (bef.)	41.26	44.28	40.31	42.56	42.1025
Insertion rate % (aft.)	99.13	99.25	99.01	99.16	99.1375
ΔInsertion rate %	57.87	54.97	58.7	56.6	57.035
HPWL(before)	5.73E+08	5.63E+08	2.84E+09	2.93E+09	
HPWL(after)	5.92E+08	5.80E+08	2.84E+09	2.98E+09	
ΔHPWL	+3.37%	+2.91%	+0.01%	+1.88%	+2.04%
Displacement	3.33E+07	3.18E+07	5.25E+07	1.10E+08	
Total movement of Vcell	1.19E+07	1.11E+07	6.24E+06	3.21E+07	
Average mov. (Row Hei.)	1.82	1.70	3.91	1.46	2.22253

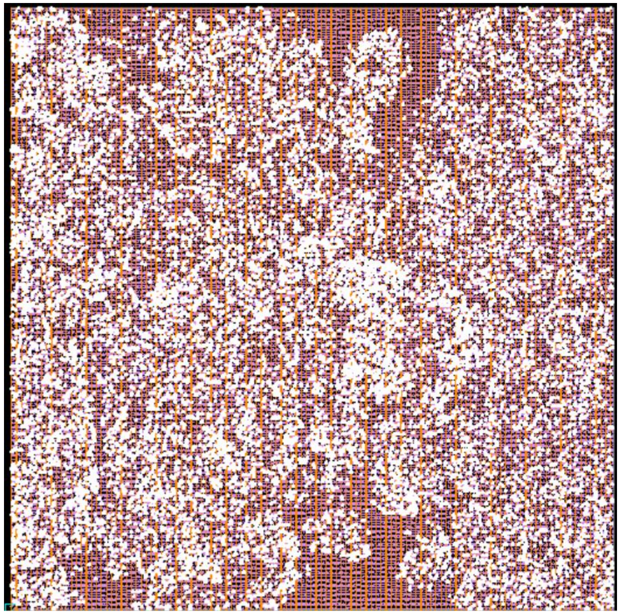
Layout of Testcases with PG Stripe

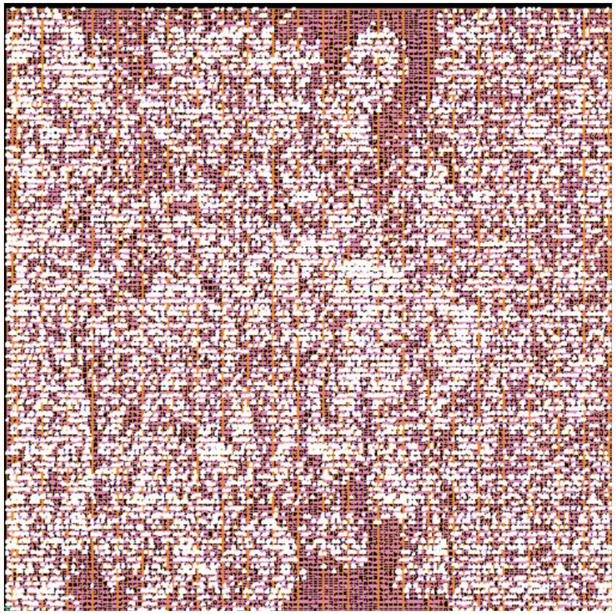
mgc_fft_1





$matrix\ mult\ 1$





Results on Testcases w/o PG Stripe

- Furthermore, we evaluate our algorithm on the testcases without impact from PG stripes

	fft_1	fft_2	des_perf_1	matrix_mult_1	Average
#Row	192	192	348	383	
#Eligible row	96	96	174	192	
#Cell	32281	32281	112644	155325	
#V-cell	3850	3832	955	13103	
Insertion rate % (bef.)	48.02	51.35	47.23	49.41	49.0025
Insertion rate % (aft.)	99.57	99.34	99.89	99.31	99.5275
ΔInsertion rate %	51.55	47.99	52.66	49.9	50.525
HPWL(before)	5.73E+08	5.63E+08	2.84E+09	2.93E+09	
HPWL(after)	5.91E+08	5.80E+08	2.82E+09	2.97E+09	
ΔHPWL	+3.30%	+2.98%	-0.69%	+1.32%	+1.73%
Displacement	4.30E+07	4.19E+07	9.85E+07	1.58E+08	
Total movement of Vcell	1.18E+07	1.11E+07	6.23E+06	3.27E+07	
Average mov. (Row Hei.)	1.80	1.69	3.90	1.49	2.22

Result on Testcases w/o Track Alignment Issue

- We evaluate our algorithm on the testcases without impact from track alignment issue

	fft_1	**fft_2**	**des_perf_1**	**matrix_mult_1**	Average
#Row	192	192	348	383	
#Eligible row	192	192	348	383	
#Cell	32281	32281	112644	155325	
#V-cell	3850	3832	955	13103	
Insertion rate % (bef.)	85.74	85.87	85.45	85.25	85.5775
Insertion rate % (aft.)	99.05	99.12	99.26	99.24	99.1675
ΔInsertion rate %	13.31	13.25	13.81	13.99	13.59
HPWL(before)	5.73E+08	5.63E+08	2.84E+09	2.93E+09	
HPWL(after)	5.68E+08	5.58E+08	2.82E+09	2.88E+09	
ΔHPWL	-0.79%	-0.97%	-0.64%	-1.56%	-1.00%
Displacement	2.39E+07	2.37E+07	8.64E+07	1.01E+08	
Total movement of Vcell	4.12E+06	4.24E+06	5.62E+06	1.10E+07	
Average mov. (Row Hei.)	0.63	0.65	3.52	0.50	1.32

CONCLUSION

Conclusion

- We propose first placement framework considering via pillar insertibility maximization in detailed placement stage.
- We explore the possible causes of insertion failure and also verified these reasons through experiments
- The experimental results show that through this algorithm, even if the solution space has been reduced by PG stripes and track alignment issue, we can still achieve a solution with high insertion rate

THANKS FOR LISTENING