ISPD 2014
Detailed Routing-Driven Placement Contest
Benchmark Design Suite A

www.ispd.cc/contests/14/ispd2014_contest.html

December 19, 2013

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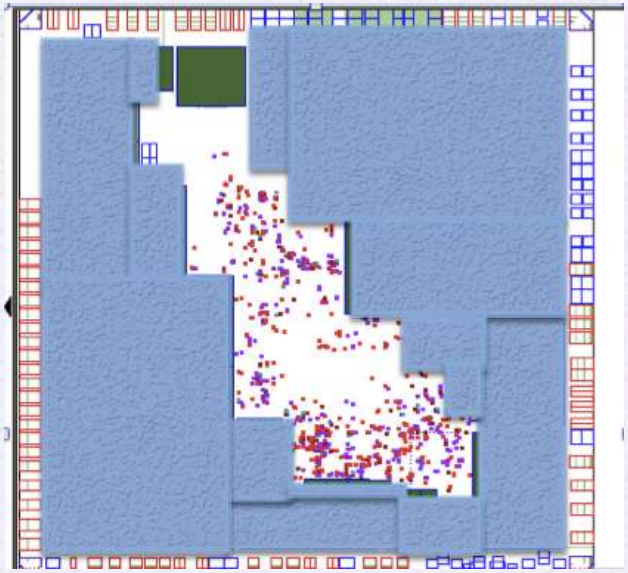
1. Motivation

Motivation

- Increasing complexity of design rules
  - miscorrelation between global routing and detailed routing
  - traditional placement approaches rendered inadequate
- Example routability challenges for placement
  - Netlist: high-fanout nets, data paths, timing objectives
  - Floorplan: placement utilization, irregular placeable area, thin channels between blocks
  - Routing constraints: blockages and restrictions by layer
  - Design rules: min-spacing, pin geometry, edge-type, end-of-line, …

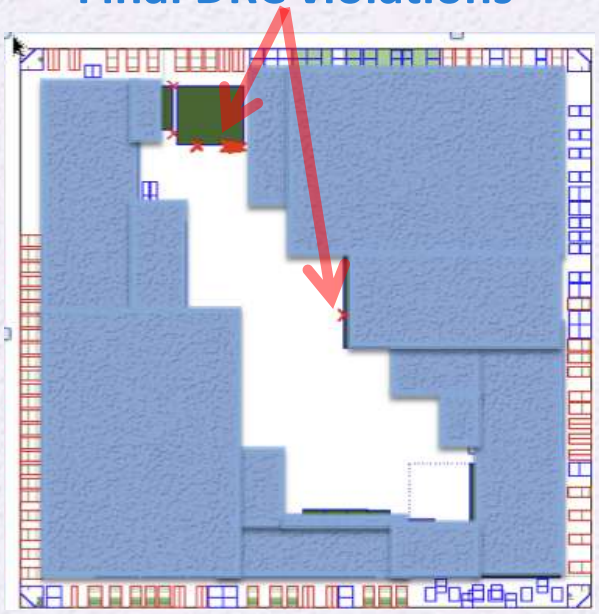
Global/Detail Routing Miscorrelation Example

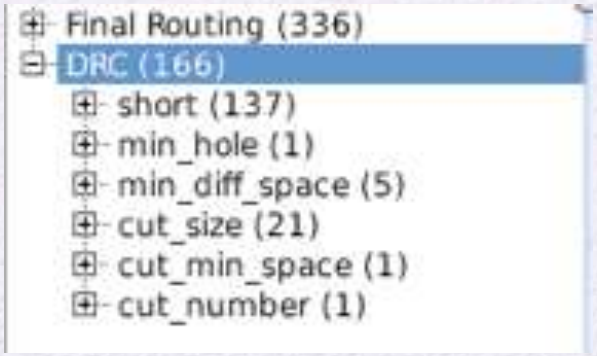
GR congestion map



	X	Y	Via	Total
Edge Count	1267068	1267137	2115090	4649295
Overflow Edges	6	0	0	6
Overflow as %	0.000129052	0	0	0.000129052
Worst	2	1	0.761905	2
Average	0.200374	0.259198	0.0434537	0.108448
Overflow Nodes	1184	48	-1	1232
Wire Length	1.24525e+11	1.21068e+11	3.85303e+06	2.45593e+11

Final DRC violations



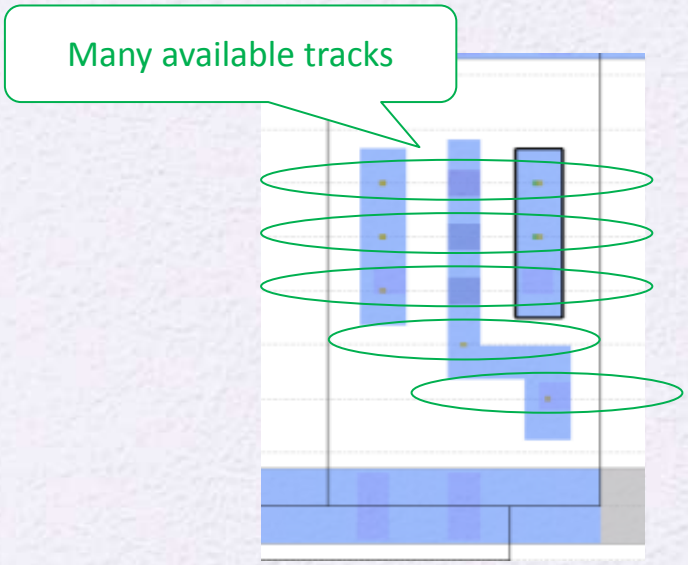


Pin Geometry Challenges

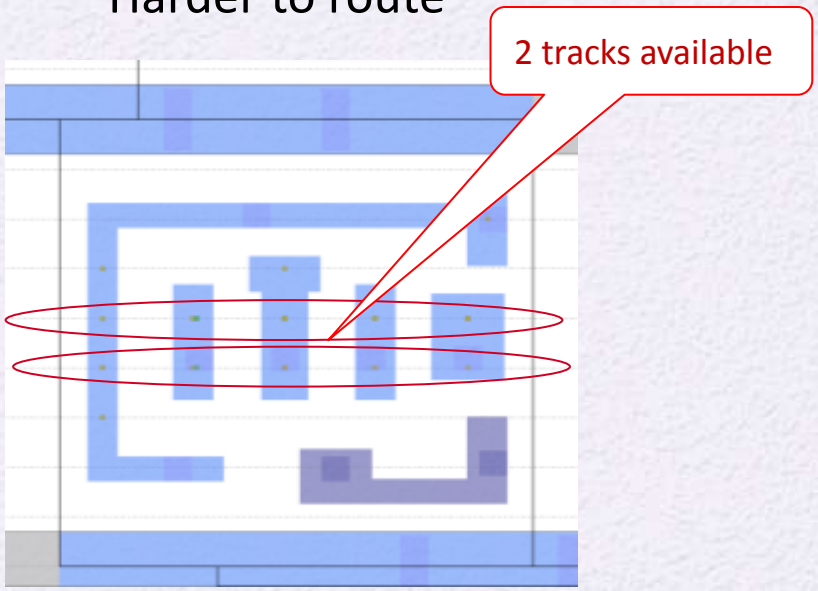
Dense metal1 pins:

- Complex DRC rules: cut space, minimum metal area, end-of-line rules, double patterning rules, etc.
- Challenging to pre-calculate routable combinations

Easy to route



Harder to route



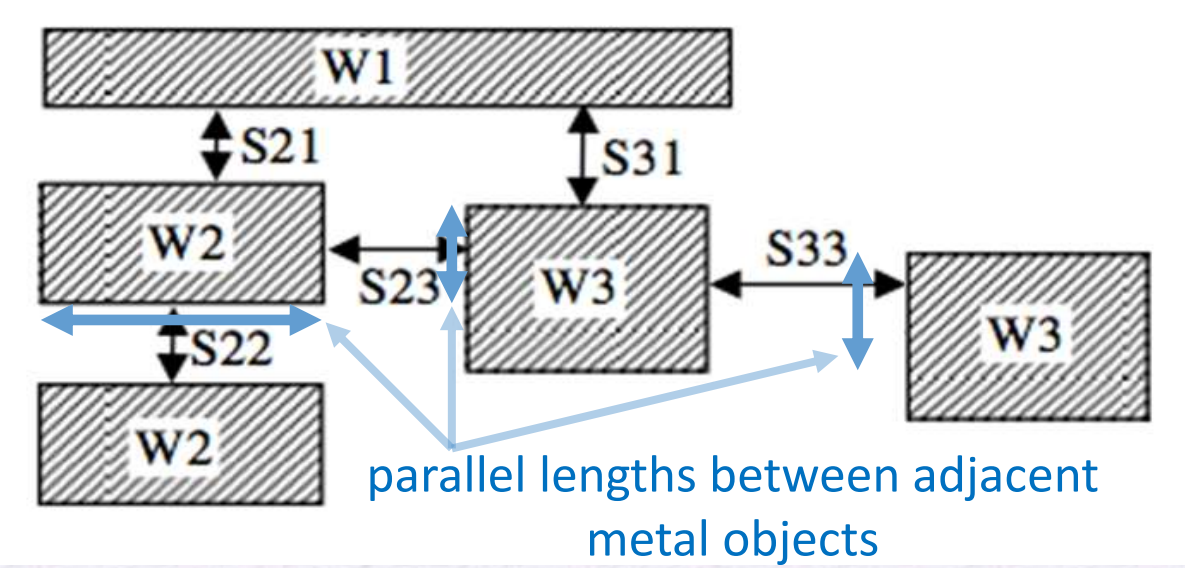
2. Sample Design Rules

Introduction to Design Rules

- For 65nm technology and below, many rules are imposed to ensure a printable GDSII mask.
- **The examples provided here are not comprehensive.** They are common on the benchmarks for this contest.
- For the LEF/DEF format specification of design rules, see www.si2.org/openeda.si2.org/projects/lefdef.

Minimum Spacing Rule

- There is a required minimum spacing between any two metal edges.
- The minimum spacing requirement depends on:
  1. The widths of the two adjacent metal objects.
  2. The parallel length between the two adjacent metal objects.

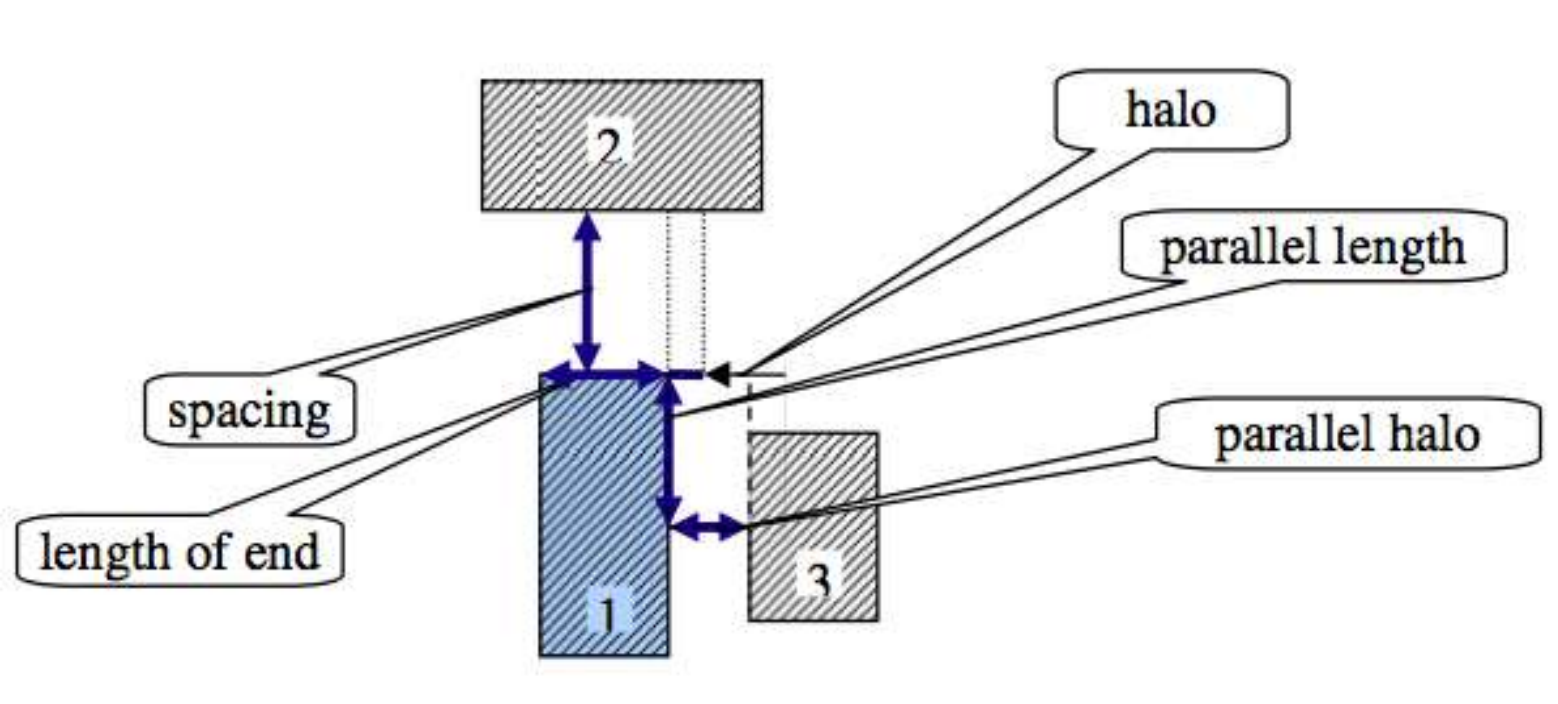


End of Line Rule

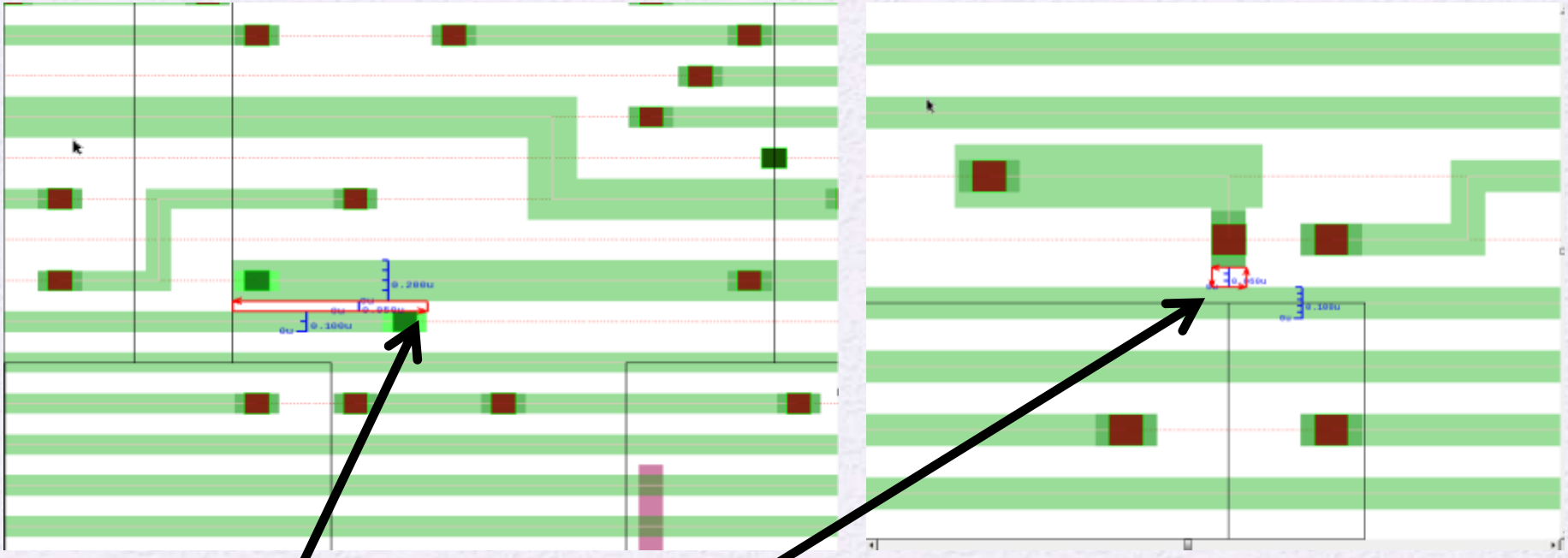
- **EOL is a spacing rule between two objects. However, more than two shapes can be involved, and various distance metrics can be used.**
- A 3-object EOL between the top of object 1 and the bottom of object 2 is illustrated on the next slide.
- EOL is a function of these four parameters:
  - **Length of end:** A minimum width for object 1 to avoid a violation.
  - **Parallel length:** Vertical distance below the top of object 1 within which object 3 will increase the minimum spacing between objects 1 and 2.
  - **Halo:** Area around corner of object 1 where object 2 may trigger EOL rule.
  - **Parallel halo:** Min spacing between object 1 and object 3 to avoid a violation.
    - *The parallel halo is an extra spacing requirement in addition to the EOL spacing.*

End of Line Parameters

EOL spacing applied to objects 1 and 2. Because object 3 overlaps the parallel length from the top of edge 1, EOL spacing between objects 1 and 2 will be required. Object 3 must remain outside the parallel halo.



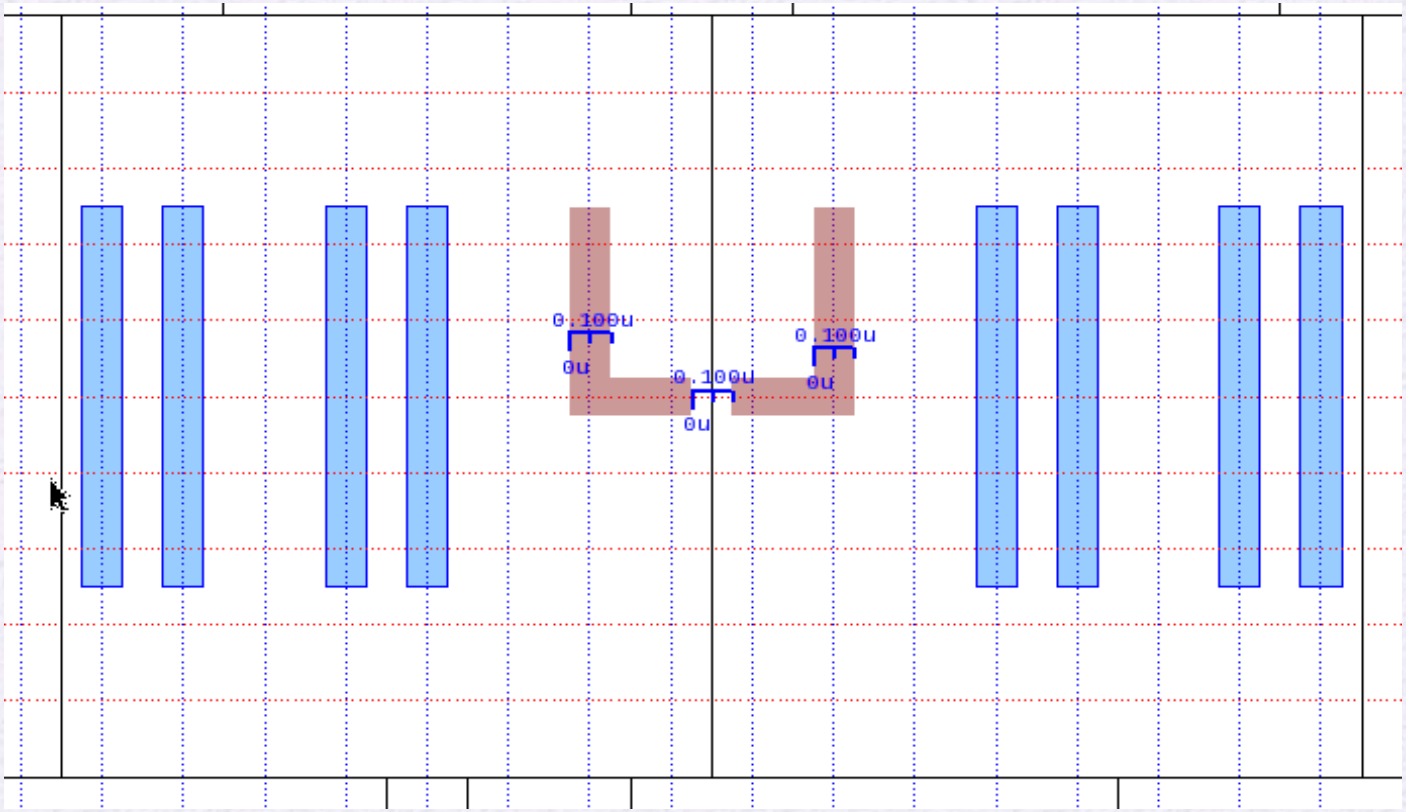
Min Spacing and End-Of-Line Spacing Violation Examples



Example **minimum spacing** and **EOL spacing** violations between routing objects within over-congested areas. Most of these violations occur in the vicinity of pins assigned with the EM_NDR non-default routing rule.

End-Of-Line Spacing Violation Example

L-shaped pin – EOL spacing violations can occur if two such cells are abutted.

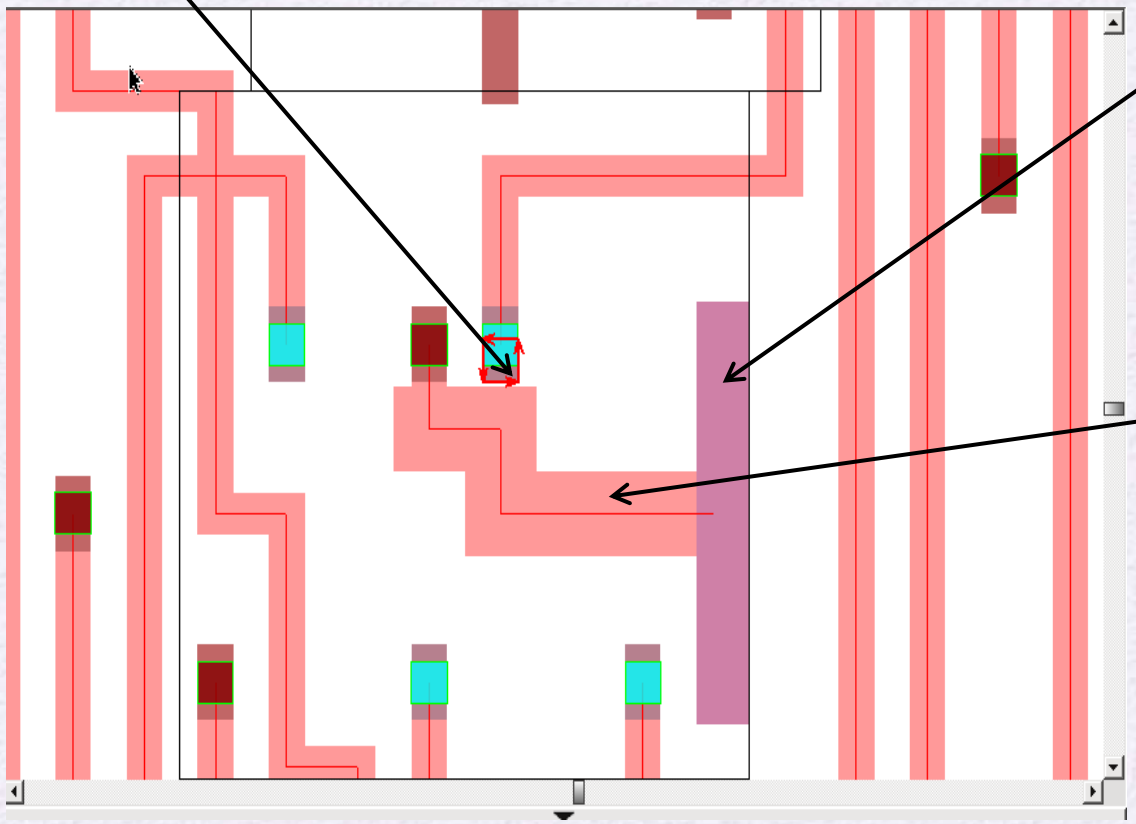


Non-Default Routing Rule (NDR)

- Non-default routing rules may specify:
  - Increased wire spacing for a net
  - Increased wire width for a net
  - Increased via cut number at selected junctions
    Cut # = number of vias connected to a wire at a single junction
- NDR may be assigned to a cell pin for wires or vias connecting to it
- NDR may or may not accompany increased pin width or specific non-rectangular pins
- NDRs are specified in the floorplan DEF file but may be assigned to a pin in the cell LEF file

Example End-of-Line Spacing Violation Due to an NDR

End-of-Line (EOL) spacing violation for routing objects within the over congested areas



Double width magenta pin with NDR assigned

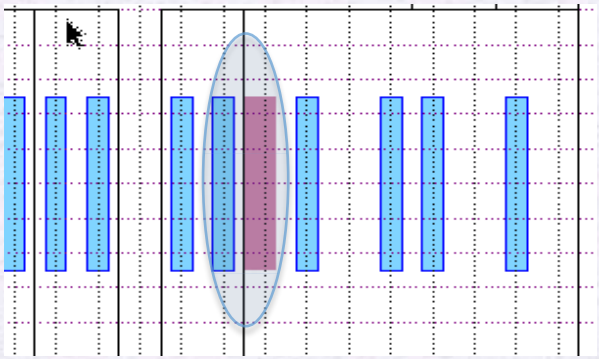
Double width wires in accordance with the NDR assigned to magenta pin

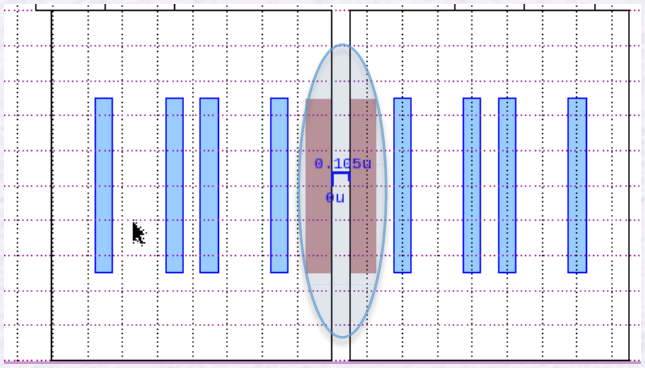
Edge-Type Rule

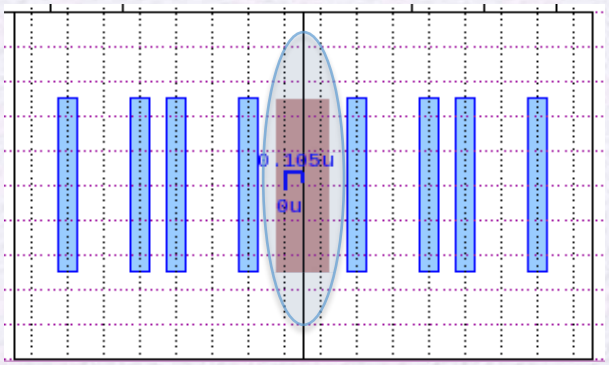
- Each **vertical edge** of a cell may have specified minimum spacings from any other vertical cell edge that can be placed right or left of it.
- They may be for yield, different implant dosages, pin reachability, etc.
- Examples:
  - The **left** edge of every ao22s01 cell must be placed at least 0.400um away from the **left** edge of every other ao22s01 cell.
  - The **left** edge of every ao22s01 cell must be placed at least 0.800um away from the **right** edge of every other a022s01 cell adjacent to it.

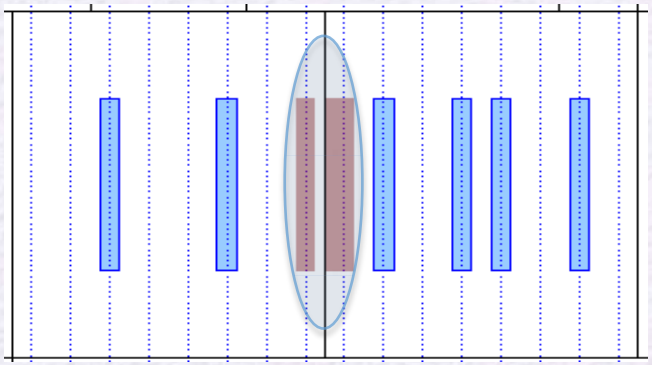
Edge-Type Spacing Violation Examples

Double width metal2 is used for the red pins.
An **edge-type** double spacing constraint is also enforced at the adjacent cell edge.
Below are four examples of violations of this:





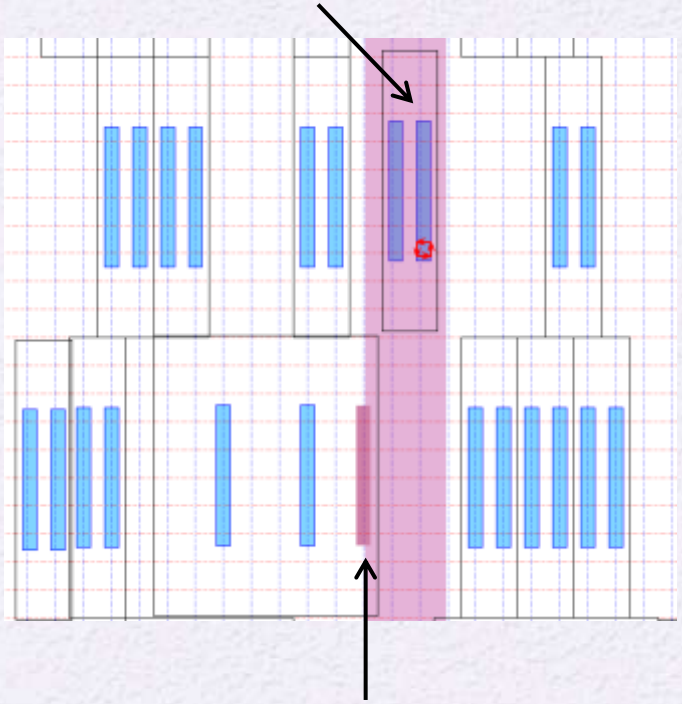




Blocked Pin Access Violation Examples

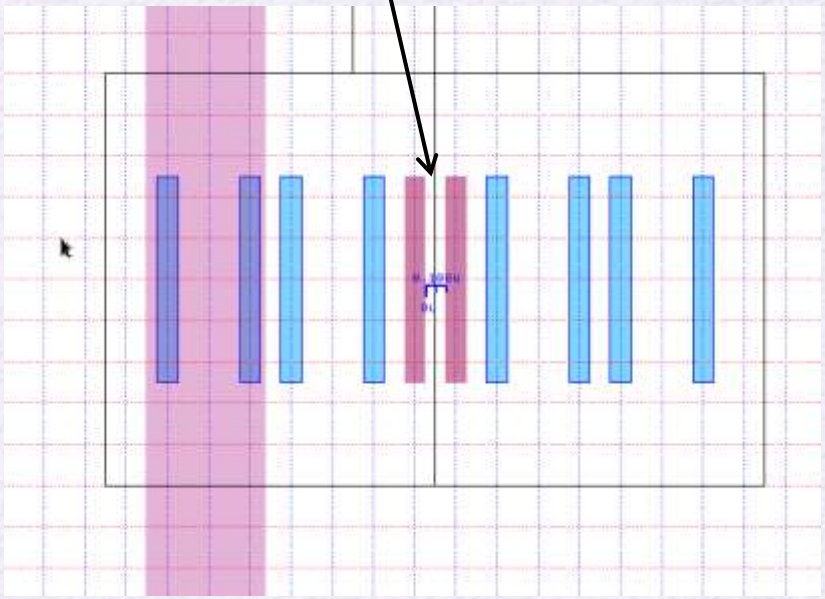
A *blocked pin* cannot be reached by a via or wire without violations.

Metal1 pins under metal2 stripe are not accessible by via1 vias



Metal2 pin overlaps metal2 stripe

Metal2 pins with EM_NDR assigned are placed too close to each other



3. Benchmark Suite A

Benchmark Source

- This benchmark suite is adapted from the ISPD 2013 gate sizing contest.
- The rectangular floorplans have no fixed or movable macros.
- Please note that we will release a second suite on January 10th adapted from the DAC 2012 routability-driven placement contest that has more complex floorplans with **fixed** macros.

Data Format

Each benchmark has four files:

- **tech.lef** (technology LEF): Physical characteristics of the routing layers, vias, placement site types, etc.
- **cells.lef** (physical LEF): Physical characteristics of the technology library for the standard cell library, macros, and I/O cells, etc.
- **floorplan.def**: Design-specific logical and physical information that represent the design during various stages of the physical design flow. This includes netlist connectivity, grouping information, physical constraints, cell locations and orientations, routing geometry data, etc.
- **design.v**: A gate-level Verilog netlist for the design.

Library Exchange Format (LEF) and Design Exchange format (DEF) 5.7 are detailed here: www.si2.org/openeda.si2.org/projects/lefdef

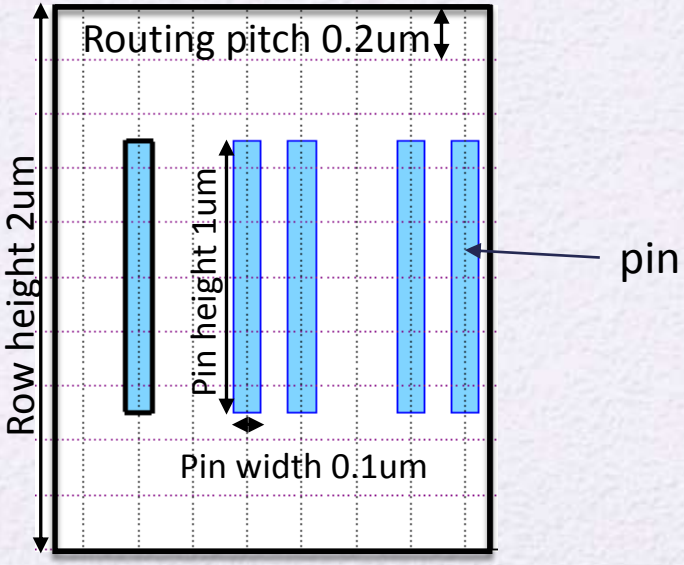
Metal Routing Layers

- There are 5 routing layers, but only 4 routing layers are available:
  metal2, metal3, metal4, and metal5.
- **Metal1 may only be used for vias to metal1 pins.**
  Metal1 is otherwise excluded from routing.
- On some designs, metal5 is also blocked to increase routing difficulty.
  - This is representative of designs where fewer routing layers are used to reduce fabrication cost.
- More conservative design rules have been added:
  min spacing, edge type, end-of-line, etc.
- **Non-default routing rules** (double width, double spacing, double cut, vias, layer restrictions) are assigned to medium fanout nets and to some cell pins.

Standard Cell Library

- Based on 65nm technology.
- The routing pitch (minimum track height) is 0.2um.
- There are 10 routing tracks per standard cell row (i.e. 2.0um tall).
- All movable cells are downsized to their minimum area.
- All movable cells are single-row high.

Example standard cell:

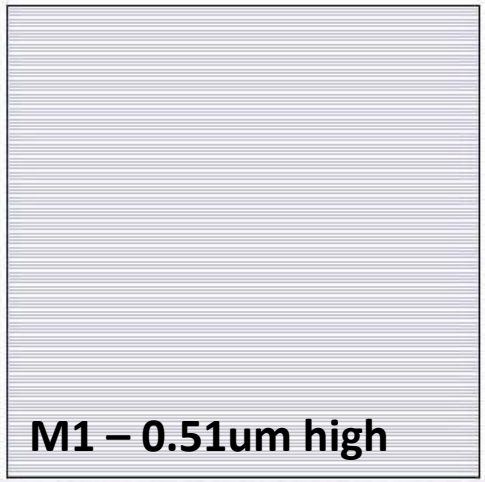


Power/Ground (PG) Mesh

- A dense PG mesh has been inserted.
- Each routing layer has uniformly spaced PG rails parallel to its preferred routing direction.
- Rail thickness is constant on each layer but varies by layer.
- PG routing-track utilization varies across layers and test cases.
  - Example edit_dist test case (placement utilization: 43%)

Metal layer	M1	M2	M3	M4	M5
PG routing track utilization	0%	6%	27%	24%	30%

Power/Ground (PG) Mesh



Spacing Rules Example in Technology LEF

```
LAYER metal2
  TYPE                  ROUTING ;
  DIRECTION             VERTICAL ;
  PITCH                 0.200 ;
  OFFSET                0.100 ;
  WIDTH                 0.1 ;
  MAXWIDTH              10.0 ;
  SPACINGTABLE
  PARALLELRUNLENGTH      0.00    0.40    0.46    1.40    4.10
  WIDTH    0.00          0.10    0.10    0.10    0.10    0.10
  WIDTH    0.30          0.10    0.12    0.12    0.12    0.12
  WIDTH    0.46          0.10    0.12    0.15    0.15    0.15
  WIDTH    1.40          0.10    0.12    0.15    0.52    0.52
  WIDTH    4.10          0.10    0.12    0.15    0.52    1.40 ;
  PROPERTY LEF57_SPACING "SPACING 0.12 ENDOFLINE 0.14 WITHIN 0.045
PARALLELEDGE 0.12 WITHIN 0.12 ;" ;
```

Edge-Type Rules Example in Technology LEF

```
PROPERTYDEFINITIONS

  LAYER LEF57_SPACING STRING ;
  LAYER LEF57_MINSTEP STRING ;
  MACRO LEF58_EDGETYPE STRING ;

  LIBRARY LEF58_CELLEDGESPACINGTABLE STRING
  "CELLEDGESPACINGTABLE
    EDGETYPE 1 2 0.400
    EDGETYPE 1 1 0.400
    EDGETYPE 2 2 0.000;" ;

END PROPERTYDEFINITIONS
```

Min-Step, Area, Minimum Cut Rules in Technology LEF

```
PROPERTY LEF57_MINSTEP "MINSTEP 0.1 MAXEDGES 1 ;" ;
AREA 0.051 ;
MINIMUMCUT 2 WIDTH 0.400 ;
MINIMUMCUT 4 WIDTH 0.720 ;
MINIMUMCUT 2 WIDTH 0.400 LENGTH 0.400 WITHIN 0.820 ;
MINIMUMCUT 2 WIDTH 2.100 LENGTH 2.100 WITHIN 2.100 ;
MINIMUMCUT 2 WIDTH 3.200 LENGTH 8.000 WITHIN 5.200 ;
```

Common Design Rules in in All Physical LEF Data

1. Most cell pins are located on metal1 layer, and are 0.5 pitches wide and 5 pitches high.
2. NDR with double wire width and double wire spacing assigned to all nets with fanout > 10.
3. Standard cell ms00f80: driving pin is promoted to metal2 layer to check ability of placement to prevent intersection with PG rails.
4. Standard cell ao22s01: output pin near edge on metal1, but has edge-type constraint with 2x spacing (0.2um).

Design Rules Variants in Physical LEF Data

5. Standard cell oa22f01: Promoted output pin “o” to metal2 and imposed 2x width, 2x spacing, 2-cut vias EM_NDR.

   This restriction should be observed within 1.0 um (i.e. 5 pitches) of the output pin, afterwards it is switched to the default rule.

   There are two variants of this rule:

   I. Double width (0.2um) for pin “o” and edge-type spacing 0.2um assigned to edge next to pin “o”, with EM_NDR double wire width and double wire spacing.

   II. Single-width L-shaped pin for “o”.

Physical LEF Data Scenarios

Based upon the design rules variants mentioned in the previous slide, there are three scenarios of physical LEF data provided in this benchmark:

- Scenario 1: cell.lef contains rules 1-4.
- Scenario 2: cell.lef contains rules 1-4 and rule 5.I.
- Scenario 3: cell.lef contains rules 1-4 and rule 5.II.

The Design Suite

- The design suite contains 8 designs adapted from the ISPD 2013 gate-sizing contest:
  - mgc_des_perf_1
  - mgc_des_perf_2
  - mgc_edit_dist_1
  - mgc_edit_dist_2
  - mgc_fft
  - mgc_matrix_mult
  - mgc_pci_bridge32_1
  - mgc_pci_bridge32_2
- Each test case is comprised of four files:

  cells.lef, design.v, floorplan.def, and tech.lef.

4. DEF Placement Requirements & Evaluation Metrics

Submitted DEF Placement Requirements

- You are expected to provide a DEF file containing the output of your placer.
- Placement legalization is recommended but not required.
- The file name must be gzipped and prepended with the design name (e.g. mgc_fft.def.gz).
- Please modify the **COMPONENTS** section of the provided **floorplan.def** file to place all **UNPLACED** cells with appropriate placement locations from your placer.

  Add the **bottom left coordinate (BLC)** of each placed cell and change

  "**+ UNPLACED**" tag to "**+ PLACED (<x_BLC> <y_BLC>) <cell orientation>**"

  Example: `- u1 INVX1 + PLACED ( 60000 20000 ) N ;`
- Changes other than to the **COMPONENTS** disqualify the submitted placement.

Evaluation Metric

- Submitted DEF placement solutions will be evaluated by the quality of their detailed routes in Mentor Graphics' Olympus-SoC™ place and route tool.
- A placement checker will check the validity of placed designs. If the submitted DEF placement is invalid, you will receive an e-mail with the respective errors.
- Valid placements will be **legalized, routed, and scored** based on cell legalization perturbations, detail routed wire length, routing violations, and design-rule check (DRC) violations.
- **Note 1:** Even though it is not part of the incremental evaluations, run time **will** be part of the final evaluation metric.
- **Note 2**: Excessive memory usage will be penalized. Memory limits for this suite will be posted later.
- **Note 3: The contest organizers may change these metrics if necessary for a fair evaluation.**

DEF Placement Validity Checker

- **A Perl script shall check that the submitted DEF placement meets the following minimum requirements:**
  - All cells must be placed within the floorplan boundary
  - No cells may be added, removed, or changed
  - Locations of fixed cells and I/O pins must not change
  - Floorplan boundary must not change
  - Net connections must not change
    - Connectivity can be omitted from the placed DEF
- **Placed DEF files that have any of these problems will not be evaluated.**
- A summary of these errors will be emailed to the contestant.
  The script is provided to contestants to check before submission.

Placement Legalization

Placement legalization will fix the following issues in submitted design.def files:

- Overlaps between cells or with blockages, and edge-type violations
- Cells not aligned on the standard cell rows
- Cells with incorrect orientation
- Cell pins that short to the PG mesh
- Blocked cell pins that are inaccessible due to the PG mesh
- DRC placement violations between standard cells

Significant cell displacement in legalization is penalized (per S_{DP} score), so we recommend minimizing such issues in your submission.

Final Placement Score

$$S = S_{DP} + S_{DR} + S_{WL} + S_{CPU}$$

- Each of the following quantities contributes to the total score:
  - *DP* : average legalization displacement of the 10% most displaced of all cells
  - *DR* : number of detailed-routing violations
  - *WL* : routed wirelength
  - *CPU* : total runtime of global placement, legalization, and routing
- A lower score is better.
- **Placements for which $DP \geq 25.25$ or $CPU \geq CPU_{max}$ are invalid, receiving the maximum score of $S = 100$.**
- Each category score except *DP* is normalized by the median unscaled score taken over all contestants' placements for the given benchmark.
- Each normalized category score is scaled to the interval [0, 25].
  - Affine scaling $f_{aff} : [a,b] \rightarrow [0, 25]$ is used for all categories except *DR*: $f_{aff}(t) = 25(t - a)/(b - a)$, where $a \leq t \leq b$.
  - Quadratic scaling is used for *DR*, as described below.

Legalization Displacement Score S_{DP}

- The raw quantity *DP* is the average Manhattan displacement of the 10% most displaced of all cells.
- Score S_{DP} is defined as follows.
  - $S_{DP} = 0$ if $DP \leq 0.25$ std-cell row heights
  - $S_{DP} = 25$ if $DP \geq 25.25$ std-cell row heights
  - Otherwise, $S_{DP} = DP - 0.25$
- In all cases, $0 \leq S_{DP} \leq 25$.
- **If $S_{DP} == 25$, then detailed routing will be skipped, and $S_{WL} = 25$, $S_{DR} = 25$, and $S_{CPU} = 25$. Placement is invalid.**

Detailed routing score S_{DR}

- Weighted sum $DR = DR(p) = w_1v_1 + w_2v_2 + w_3v_3 + w_4v_4$ is computed from the number of violations v_i of routing violation type i and weight w_i in the table below.
- Let DR_{med} denote the median of these unscaled sums DR over valid placements p.
- If $DR/(1+DR_{med}) > 100$, then $S_{DR} = 25$.
- Otherwise, $\boldsymbol{S_{DR} = 2.5\,(DR/(1+DR_{med}))^{1/2}}$. In all cases, $0 \le S_{DR} \le 25$.

  Square root is taken, as there may be a wide range in violation counts.

Design Violation Type	Weighting w_i
Routing open	1.0
Routing blocked pin	1.0
Routing short	1.0
Design rule check (DRC) violation	0.2

Detail-Routed Wirelength Score S_{WL}

- Unscaled score *WL* is simply the final detail-routed wirelength reported by the router.
- Over all valid placements *p* on a benchmark with $S_{DP}(p) < 25$, let
  - WL_{med} = the median of the *WL(p).*
  - WL_{min} = the minimum of the *WL(p).*
- If $WL \geq 5 \times WL_{med}$, then $S_{WL} = 25$.
- Otherwise, $S_{WL} = f_{aff}(WL / WL_{med})$, where f_{aff} denotes affine scaling from $[WL_{min} / WL_{med}, 5]$ into [0, 25].

Run-time Score S_{CPU}

- Let *CPU* = total wall-clock time for placement, legalization, global and detailed routing on one benchmark, on an unloaded machine with 8 cores.
- Each benchmark suite has a hard run-time limit per test case, CPU_{max}.
  - Benchmark Suite A: **CPU_{max} = 24 hrs per test case**
- **If $CPU > CPU_{max}$, then $S_{CPU} = 25$, $S_{DP} = 25$, $S_{DR} = 25$, $S_{WL} = 25$, and $S = 100$.**
- Over all valid placements *p* on the benchmark with $CPU(p) < CPU_{max}$, let CPU_{min} = minimum of the $CPU(p)$ and CPU_{med} = median of the $CPU(p)$.
- $S_{CPU} = f_{aff}(CPU / CPU_{med})$, where f_{aff} denotes affine scaling from $[CPU_{min} / CPU_{med}, CPU_{max} / CPU_{med}]$ into [0, 25].

5. DEF Placement Submission Procedure

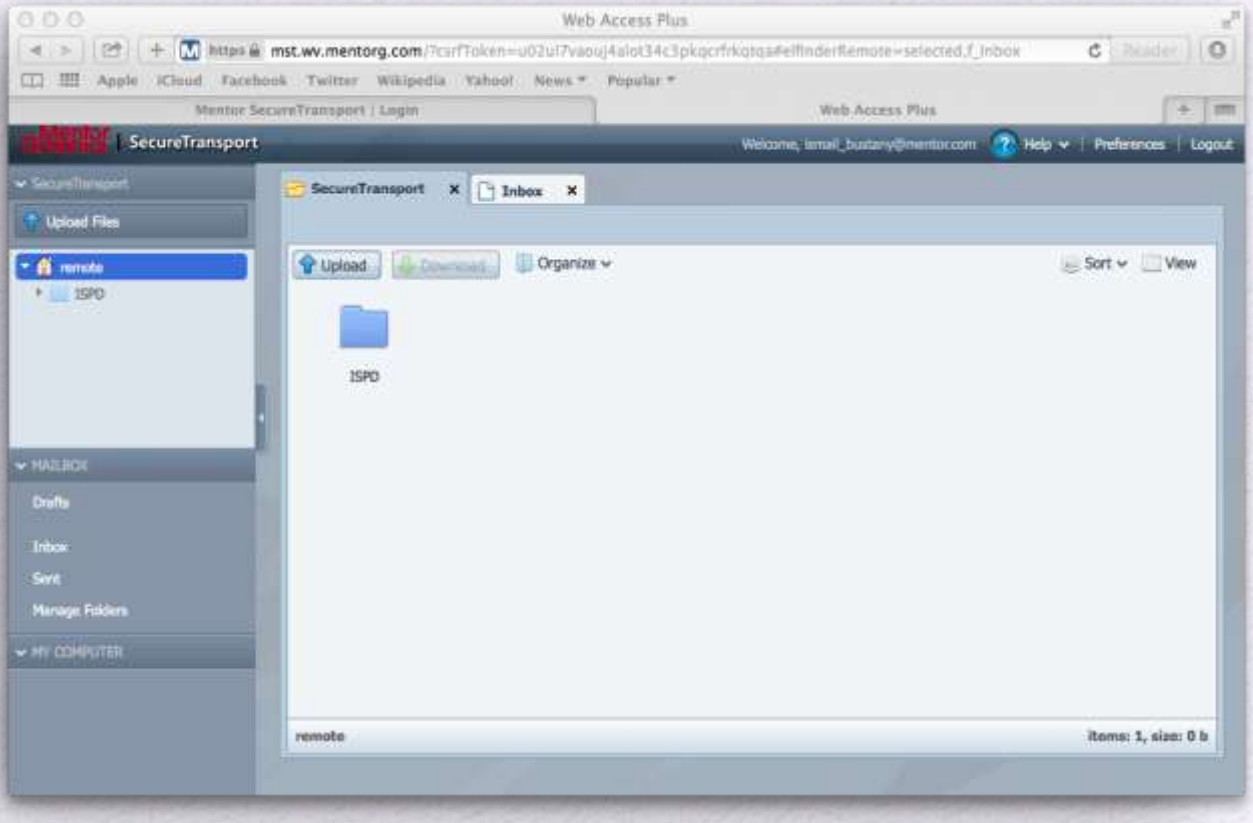
DEF Placement Submission Procedure

1. Please visit **https://mst.mentorg.com/**

2. Login using your support-net account email and password. If you do not have a support-net account, please e-mail **ispd2014contest@gmail.com**.

DEF Placement Submission Procedure

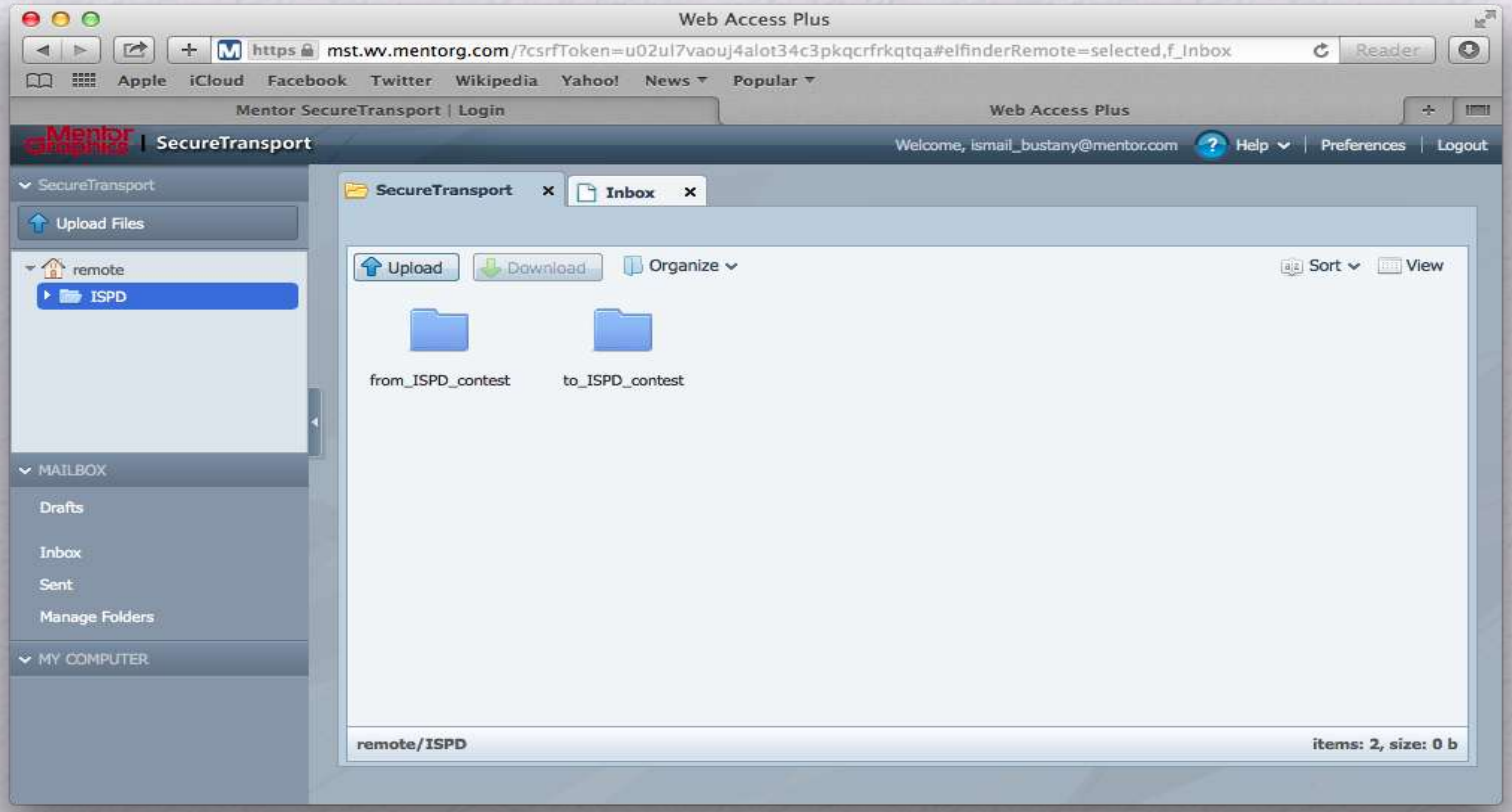
3. Once logged in, you will see the following screen:



4. Click open the ISPD folder.

DEF Placement Submission Procedure

5. You will see two folders: **from_ISPD_contest** and **to_ISPD_contest**:



5. Upload your DEF placement to the to_ISPD_contest folder.
Please use the design name appended by .def.gz (e.g. mgc_fft.def.gz). Gzip compressed files are required.

DEF Placement Submission Procedure

7. Your gzipped DEF placement file will be processed. You will be notified by e-mail once the evaluation result is ready to view.

8. If the placement file is invalid an error log will be copied to the from_ISPD_contest folder; otherwise, a tar gzipped output file will be copied there.

9. Upon e-mail notification, please log in to mst.wv.mentorg.com. You can download a gzipped tar output file in the from_ISPD_contest folder.

Note: There will be a limit on the number of submissions per day. Currently, it is 8 submissions per day. This may be adjusted depending on the server load. Updates will be posted on the contest website.

6. Contacts

Contact Information

- Please e-mail any benchmark-related questions to
  ispd2014contest@gmail.com

Contest Organizers

Mentor Graphics Corporation

- Ismail Bustany – contest chair
- Vladimir Yutsis
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8. References

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