ISPD 2012 Discrete Gate Sizing Contest

Speakers: Mustafa Ozdal , Cheng Zhuo

Organizers: Gustavo Wilke, Steve Burns, Andrey Ayupov, Chirayu Amin

Intel Corporation, Hillsboro OR

People

Contest Organizers	Responsibilities
Cheng Zhuo	Communications + *evaluations*
Gustavo Wilke	Final evaluations
Steve Burns	Cell library
Andrey Ayupov	Benchmarks
Chirayu Amin	Timing
Mustafa Ozdal	Contest organization + *parsers*

Special Thanks To:

- *Troy Wood, Robert Hoogenstryd (Synopsys) ;*
- *Noel Menezes, Jason Xu, Alaena Young, Nanda Kuruganti, Shishpal Rawat, and Robert Nguyen (Intel);*

Participation Statistics

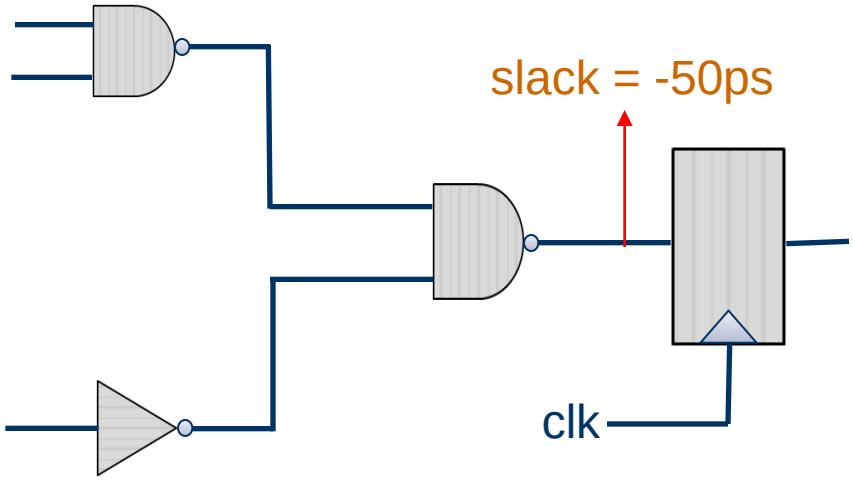
- 32 initial registrations
  - Asia: 15 teams
  - North America: 13 teams
  - South America: 2 teams
  - Europe: 2 teams
    - *Overall 8 different countries*
- 22 alpha binary submissions
- 18 final submissions

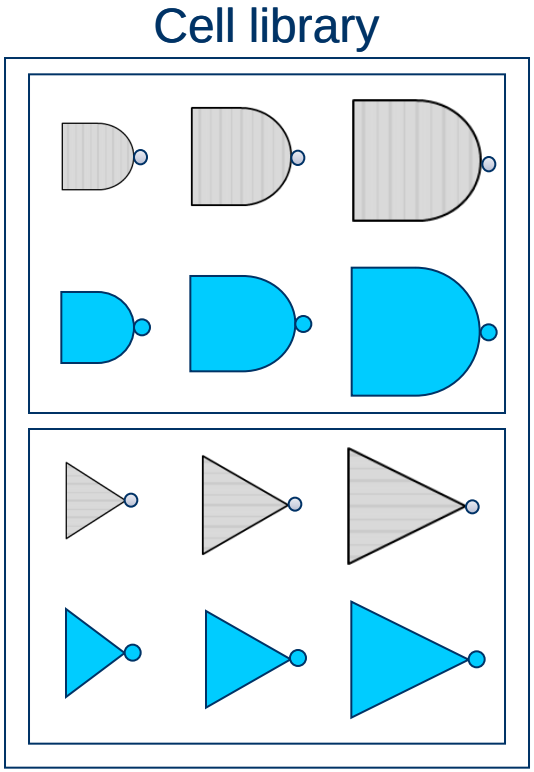
ISPD 2012 Contest Overview

Discrete Gate Sizing Contest: An Overview

- Simultaneous gate sizing and Vt assignment to optimize power under performance constraints
- Problem formulation:
  - Inputs:
    - Standard cell library
    - Netlist
    - Timing constraints
    - Interconnect parasitics
  - Outputs:
    - Cell sizes and types
  - Objective:
    - Satisfy all performance constraints
    - Minimize total leakage power
- An industrial timing engine used as the reference timer

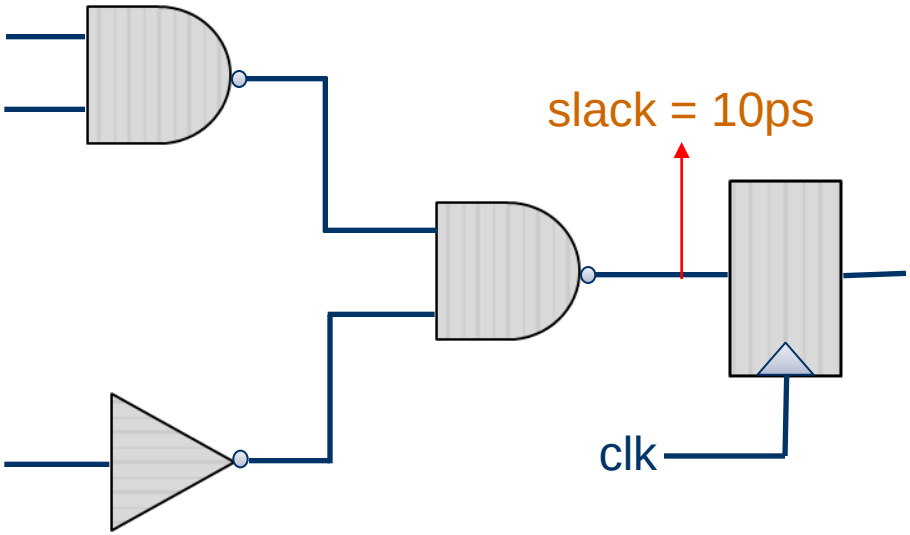
Gate Sizing and Threshold Voltage Selection

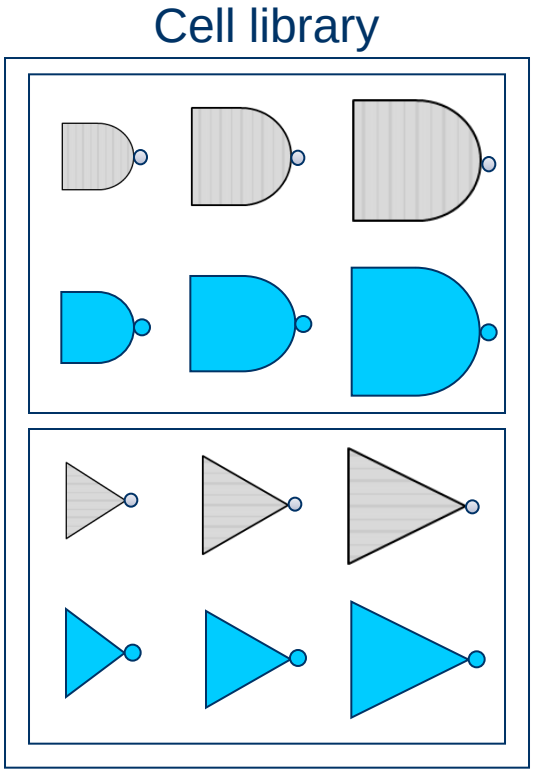




- Choose the cell sizes and device types from the library such that:
  - All timing constraints are satisfied
  - Total power is minimized

Gate Sizing and Threshold Voltage Selection





- Choose the cell sizes and device types from the library such that:
  - All timing constraints are satisfied
  - Total power is minimized

Contest Objectives

- Main objective: *Expose industrial challenges in the gate sizing problem to academia*

- Common industrial challenges:
  - Discrete cell sizes
    - Continuous optimization + rounding: typically suboptimal
  - Non-convex cell timing models
    - Due to transistor folding in the layout, etc.
  - Slew dependencies and constraints
  - Large design sizes

  } captured in the contest

  - Complex timing constraints
    - Multiple clock domains, false paths, interconnect models

  } not captured in the contest

Benchmark Features

- Each benchmark circuit consists of:
  - A netlist
    - Structured verilog format
    - Sanitized (no hierarchy, no buses, no unconnected pins, etc.)
  - Interconnect parasitics
    - IEEE SPEF format
    - Lumped capacitance
    - Zero resistance
  - Timing constraints
    - Synopsys Design Constraints (SDC) format
    - Single clock period, no false paths, no latches
    - Circuit interface (driving cells at PIs, loads at POs, etc.)
- Standard industrial formats
- C++ parser helpers provided by the organizers

Benchmarks Statistics

- Sample benchmarks made public before the contest

Name	# I/O pins	# Comb cells	# Seq Cells	# Total Cells
usb_phy	34	514	98	612
DMA	959	23K	2K	25K
pci_bridge32	361	30K	3K	33K
des_perf	374	102K	9K	111K
vga_lcd	184	148K	17K	165K
b19	47	213K	7K	219K
leon3mp	333	540K	109K	649K
leon2	700	645K	149K	794K
netcard	1,846	861K	98K	959K

All netlists derived from the IWLS-2005 benchmarks

Contest Benchmarks

- Semi-blind evaluations
  - Released: All netlists
    - To avoid potential issues due to unknown circuit topologies, verilog naming conventions, etc.
  - Kept secret: Timing constraints and parasitics
    - To prevent excessive tuning
- 14 benchmarks used for evaluations
  - 7 netlists
  - 2 different clock periods for each netlist (fast and slow)

Standard Cell Library

- Cell library created specifically for this contest
  - Realistic non-convex timing models
  - Realistic discrete levels
- 11 combinational functions + 1 flip flop
- For each combinational cell family:
  - 30 different cell types/sizes:
    - 3 threshold voltages (Vt)
    - 10 sizes for each Vt
- Synopsys Liberty™ format with lookup tables for delay and slew

Cell Library: Delay and Slew Tables

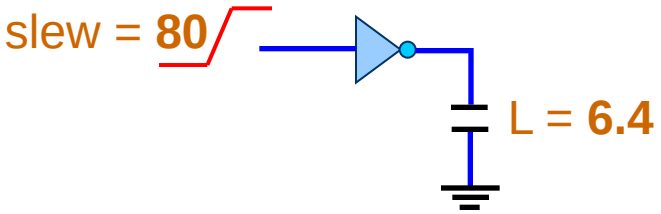
Delay and output slew defined as a function of input slew and output loads

	5	30	50	80	140	200	300	500
0.0	26	31	35	41	53	65	85	125
0.8	30	35	39	45	57	69	89	129
1.6	34	39	43	49	61	73	93	133
3.2	42	47	51	57	69	81	101	141
6.4	58	63	67	73	85	97	117	157
12.8	90	95	99	105	117	129	149	189
25.6	154	159	163	169	181	193	213	253

input slews

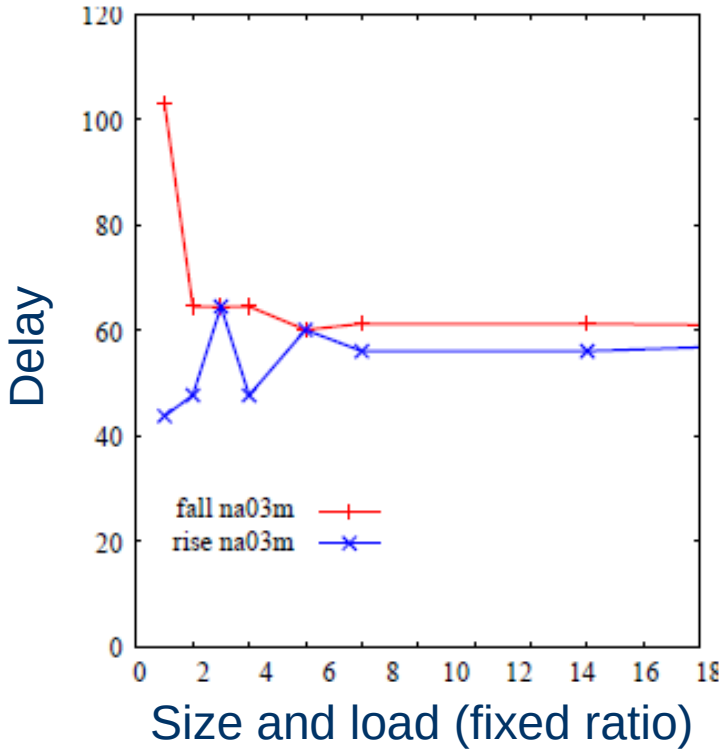
delay table

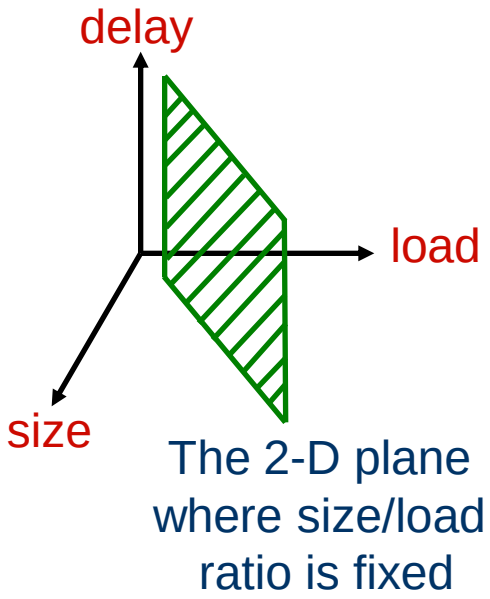
output loads



Cell Library: Timing Models

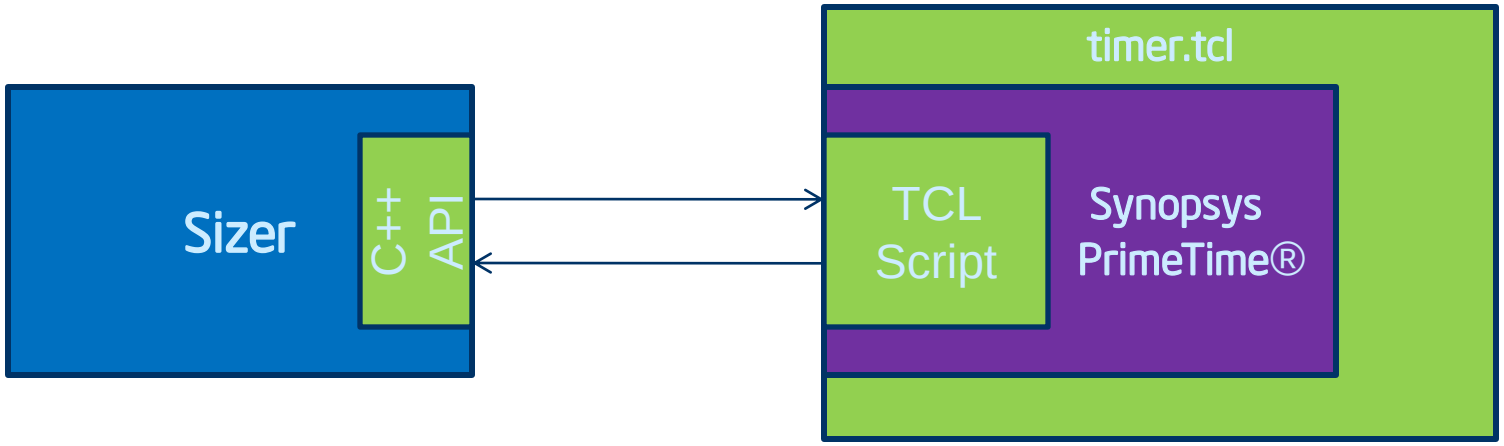
- Timing tables generated based on a simple current source model
- Two main sources of non-convexities:
  - Transistor folding in the layout
  - p/n transistor size ratios not always constant due to discreteness





Timing Infrastructure

- Synopsys PrimeTime® used for final evaluations
- Contestants had two choices:
  - Implement own STA
  - Make calls to Synopsys PrimeTime® from sizer
- Optional timing infrastructure provided



Special thanks to Troy Wood and Robert Hoogenstryd from Synopsys for providing academic licenses to Synopsys PrimeTime® and valuable support!

ISPD 2012 Contest Evaluation

Contest Evaluation

- Basic evaluation metrics
  - Violations
  - Power
  - Runtime
- Two separate rankings
  - Primary: Quality
  - Secondary: Tradeoff between quality and run time

Evaluation Metrics: Violations

- Violations are divided into three different types
  - Negative slack (ps)
    - Sum of violations at PO and sequential inputs
  - Slew (ps)
    - Sum of violations at PO and cell input pins
  - Maximum capacitance (fF)
    - Sum of violations at cell output pin
- All benchmarks can be sized without any violations

Evaluation Metrics: Power

- Only leakage power is considered
- Total leakage power value is given by the sum of the leakage power for each cell

Evaluation Metrics: Runtime

- Runtime is the wall clock time from the beginning to the end of the execution of the submitted binary
- All jobs running after the runtime limit is reached will be killed

$$Runtime\ limit = 5h + 1h \times Roundup\left(\frac{\#\,gates}{35K}\right)$$

- Machine specification
  - 2 × 6-core Intel Xeon X5675 with 96GB RAM
    - 12 cores available for parallel execution

Primary Metric: Quality

- The ranking metric for a benchmark is defined in lexicographic order as:
  - First: ∑violations
  - Second: ∑power (when violations are tied)
  - Third: Runtime (when violations and power are tied)
- Sum of the ranks for each benchmark defines the final score for each team
  - **The lowest rank sum wins the contest!**

Secondary Metric: Quality/Runtime

- Encourage multi-threading and optimization efficiency
- All the solutions with the same number of violations are ranked by:

$$cost = \frac{Power}{Power_{REF}} + 0.05\frac{Runtime}{Runtime_{REF}}$$

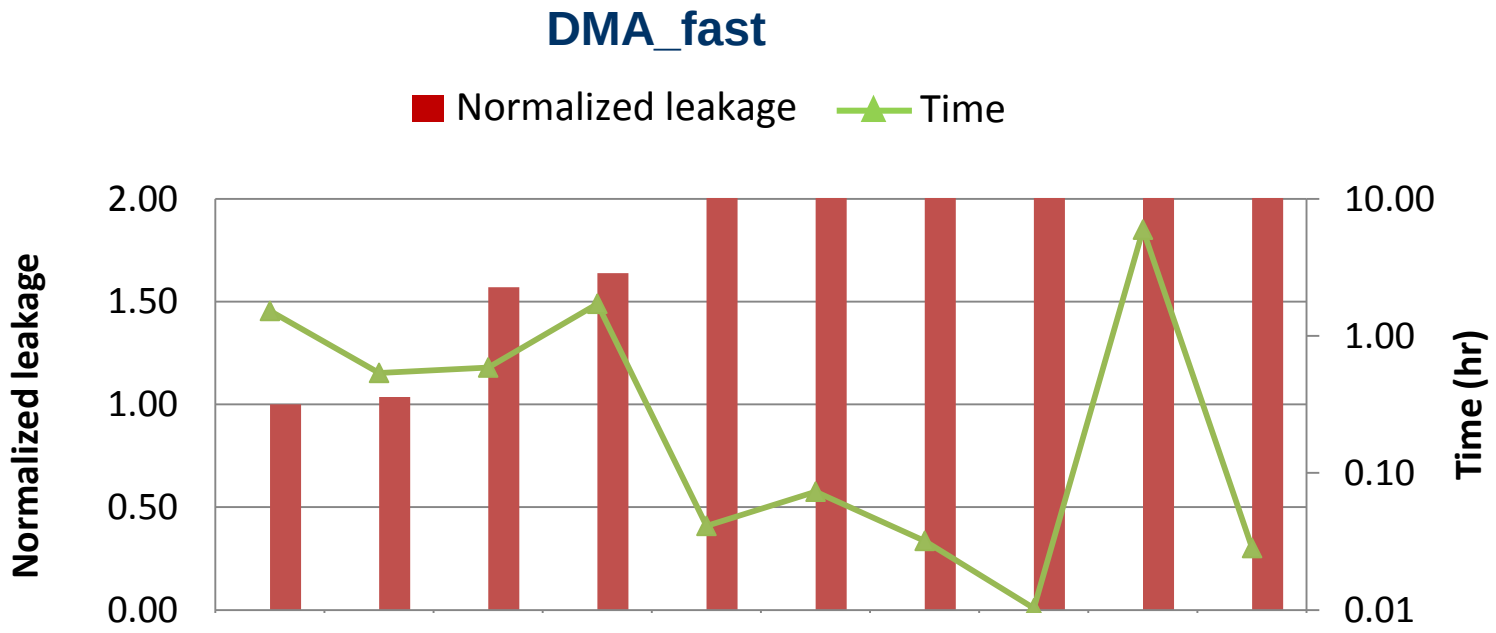
  - 1% degradation in the solution quality can be compensated by a 20% runtime reduction
  - The reference values are from the best quality solution for each benchmark

ISPD 2012 Contest Results

Contest Awards

- Recognition and cash prizes for:
  - Top three teams in the primary metric
  - Top team in the secondary metric

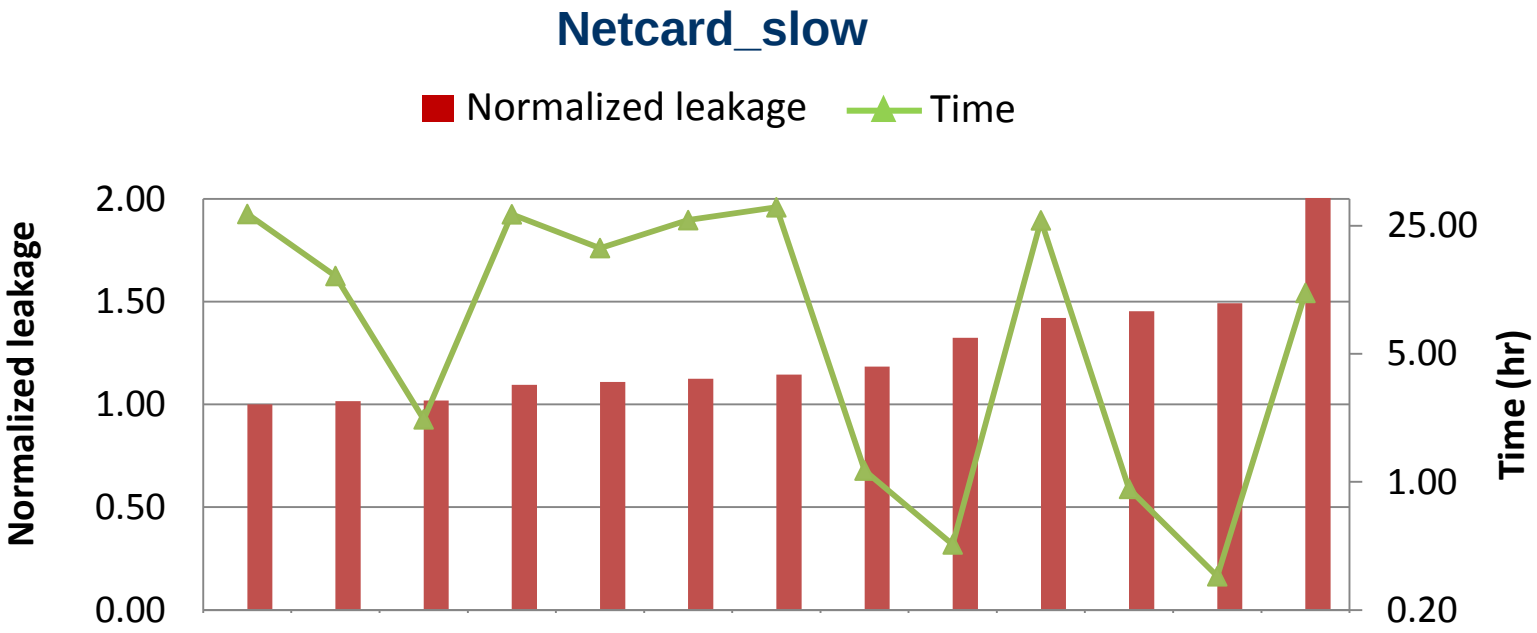
Results Comparison: Small but Difficult



leakage (W)	0.31	0.32	0.49	0.51	0.69	0.74	0.86	0.97	1.01	2.98
Normalized leakage	1.00	1.04	1.57	1.64	2.21	2.37	2.75	3.10	3.25	9.55
time (hr)	1.52	0.54	0.59	1.72	0.04	0.07	0.03	0.01	5.98	0.03

- 10 out of 18 teams completed without violations

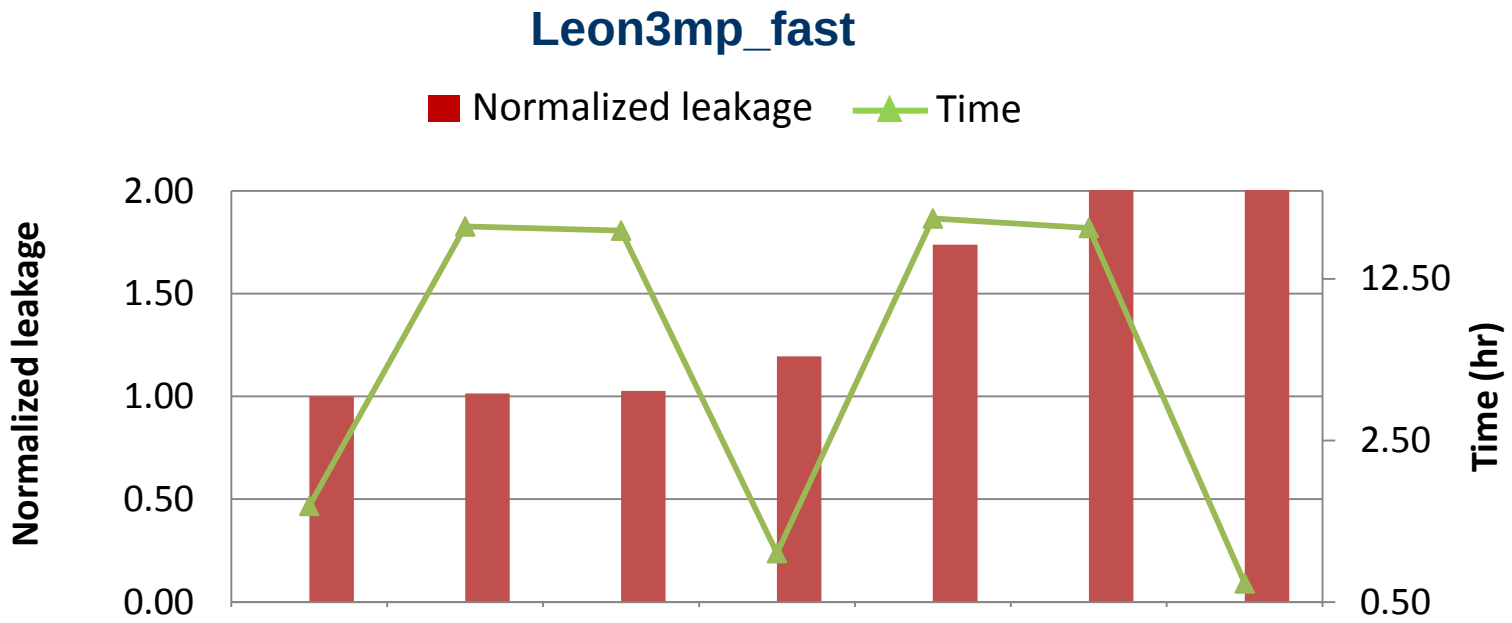
Results Comparison: Large but Easy



leakage (W)	1.77	1.80	1.81	1.94	1.97	2.00	2.03	2.10	2.35	2.52	2.58	2.65	77.6
Normalized leakage	1.00	1.02	1.02	1.10	1.11	1.12	1.14	1.18	1.33	1.42	1.45	1.49	43.7
time (hr)	29.0	13.3	2.20	28.8	18.8	26.8	31.5	1.15	0.46	26.7	0.92	0.31	10.7

- 13 out of 18 teams completed without violations

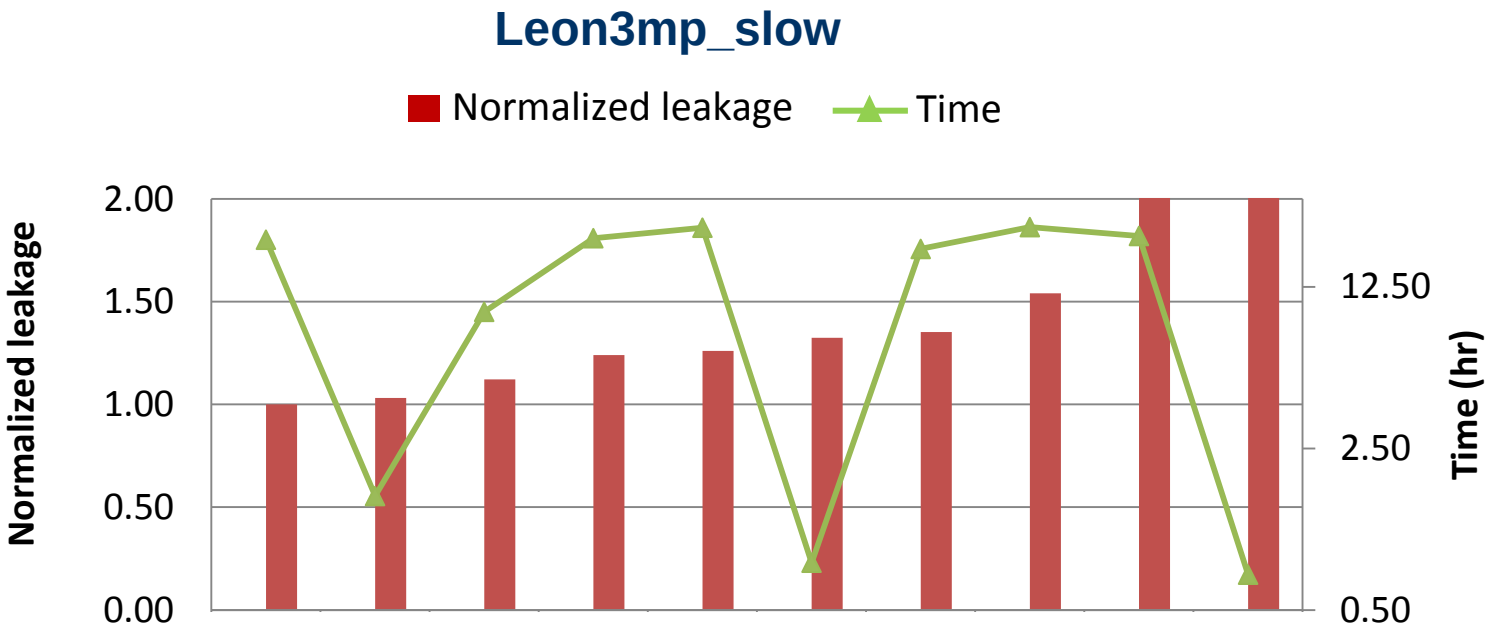
Results Comparison: Fast vs Slow



leakage (W)	2.02	2.05	2.08	2.42	3.51	4.94	5.80
Normalized leakage	1.00	1.01	1.03	1.20	1.74	2.45	2.87
time (hr)	1.30	21.07	20.22	0.81	22.81	20.76	0.60

- 7 out of 18 teams completed without violations

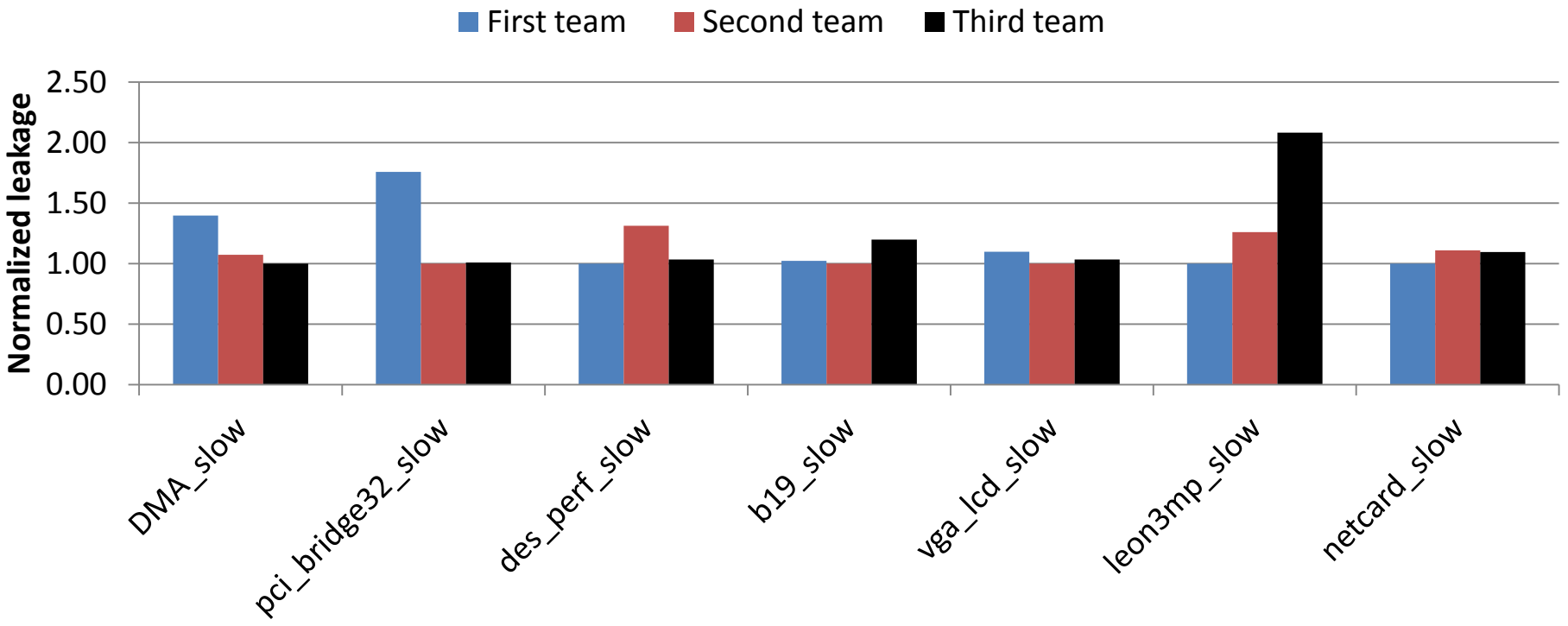
Results Comparison: Fast vs Slow



leakage (W)	1.42	1.47	1.59	1.76	1.79	1.88	1.92	2.19	2.96	3.82
Normalized leakage	1.00	1.03	1.12	1.24	1.26	1.33	1.35	1.54	2.08	2.69
time (hr)	20.00	1.56	9.75	20.30	22.54	0.80	18.24	22.68	20.76	0.71

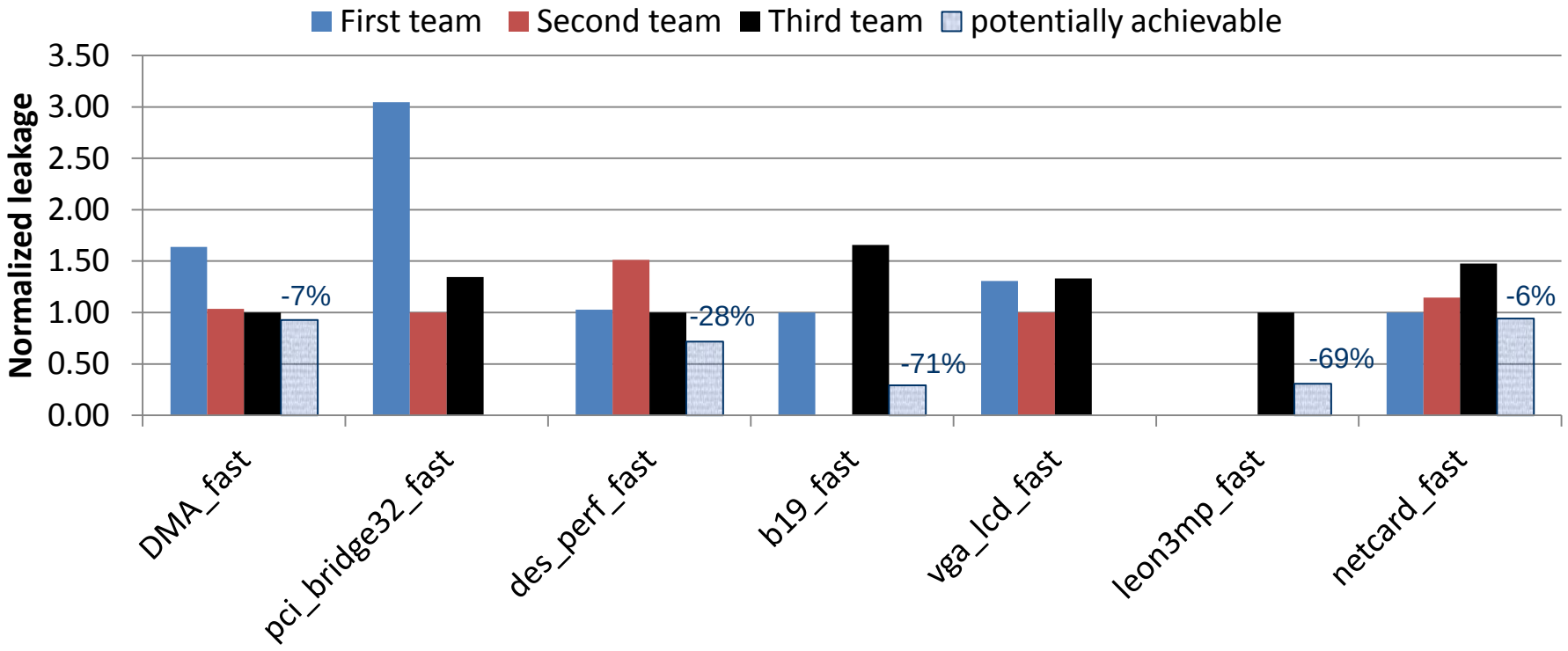
- 10 out of 18 teams completed without violations

Primary Ranking: Winner Teams



- Performance of the winner teams for the benchmarks with slow constraints
  - No violations found for all the three teams

Primary Ranking: Winner Teams



- Performance of the winner teams for the benchmarks with fast constraints
  - First team has violation for leon3mp_fast
  - Second team has violation for b19_fast and leon3mp_fast

Primary Metric: Detailed Ranking

Ranks of the top 3 teams for each benchmark			
Benchmark	First team	Second team	Third team
Vga_lcd_slow	4	1	2
Vga_lcd_fast	3	1	5
Pci_bridge_slow	4	1	2
Pci_bridge_fast	6	1	2
netcard_slow	1	5	4
netcard_fast	1	3	7
leon3mp_slow	1	5	9
leon3mp_fast	9	11	6
DMA_slow	3	2	1
DMA_fast	4	2	1
des_perf_slow	1	3	2
des_perf _fast	2	4	1
b19 _slow	2	1	4
b19_fast	7	12	9
Sum	**48**	**52**	**55**

Primary Metric: 3rd Place Winner

- Team name: PowerValve
- Affiliation: National Tsing Hua University and Missouri University of S&T
- Team members: Chung-Han Chou, Chi-Hsuan Lin, Kuan-Yu Lai, Rui-Xiang Xu, Yi-Chiao Chen,Yiyu Shi, Shih-Chieh Chang

Primary Metric: 2nd Place Winner

- Team name: UFRGS-BRAZIL
- Affiliation: Universidade Federal do Rio Grande do Sul
- Team members: Tiago Reimann, Guilherme Flach, Gracieli Posser, Jozeanne Belomo, Marcelo Johann, Ricardo Reis

Primary Metric: 1st Place Winner

- Team name: NTUgs
- Affiliation: National Taiwan University
- Team members: Kuan-Hsien Ho, Po-Ya Hsu, Yu-Chen Chen, Yao-Wen Chang

Secondary Metric: 1st Place Winner

- Team name: UFRGS-BRAZIL
- Affiliation: Universidade Federal do Rio Grande do Sul
- Team members: Tiago Reimann, Guilherme Flach, Gracieli Posser, Jozeanne Belomo, Marcelo Johann, Ricardo Reis

Primary Metric: Top 6

Name	Affiliation	Members	Score
NTUgs	National Taiwan University	Kuan-Hsien Ho, Po-Ya Hsu, Yu-Chen Chen, and Yao-Wen Chang	48
UFRGS-BRAZIL	Universidade Federal do Rio Grande do Sul	Tiago Reimann, Guilherme Flach, Gracieli Posser, Jozeanne Belomo, Marcelo Johann, Ricardo Reis	52
PowerValve	National Tsing Hua University and Missouri University of S&T	Chung-Han Chou, Chi-Hsuan Lin, Kuan-Yu Lai, Rui-Xiang Xu, Yi-Chiao Chen, Yiyu Shi, Shih-Chieh Chang	55
Goldilocks	University of Michigan	Myung-Chul Kim, Jin Hu, Igor L. Markov	77
eOPT	New Mexico State University	Mustafa Aktan, Vishal Nawathe, Vojin G. Oklobdzija	88
CUsizer	The Chinese University of Hong Kong	Tao Huang, Wing-Kai Chow, Yuan Jiang, Evangeline F. Y. Young	92

Secondary Metric: Top 6

Name	Affiliation	Members	Score
UFRGS-BRAZIL	Universidade Federal do Rio Grande do Sul	Tiago Reimann, Guilherme Flach, Gracieli Posser, Jozeanne Belomo, Marcelo Johann, Ricardo Reis	51
NTUgs	National Taiwan University	Kuan-Hsien Ho, Po-Ya Hsu, Yu-Chen Chen, and Yao-Wen Chang	58
PowerValve	National Tsing Hua University and Missouri University of S&T	Chung-Han Chou, Chi-Hsuan Lin, Kuan-Yu Lai, Rui-Xiang Xu, Yi-Chiao Chen, Yiyu Shi, Shih-Chieh Chang	61
Goldilocks	University of Michigan	Myung-Chul Kim, Jin Hu, Igor L. Markov	71
eOPT	New Mexico State University	Mustafa Aktan, Vishal Nawathe, Vojin G. Oklobdzija	82
CUsizer	The Chinese University of Hong Kong	Tao Huang, Wing-Kai Chow, Yuan Jiang, Evangeline F. Y. Young	91

Technical Survey for the Contest

- A non-mandatory tech survey to all the teams after the contest
  - Major optimization algorithm
  - Discrete or continuous optimization
  - Utilization of multiple cores
  - Timing engine implementation
  - Cell timing models (lookup vs analytical)
- 10 out of 18 teams participated

Survey Results

- Diversity in the algorithms:
  - Network flow, dynamic programming, simulated annealing, Lagrangian relaxation, heuristics, and hybrid approaches
- 90% of the teams use discrete optimization
- 60% of the teams use multiple threads
  - Obtain more than 2-4X speed up for 4-8 threads
  - At least 2 out of top 6 winners use multi-threads
- 80% of the teams use their own timer instead of the reference timer
- 90% of the teams use the library look-up tables directly instead of analytical model fitting

Thank you!

BACKUP SLIDES

Leakage for the Top 6 Winners of Primary Metric

Leakage data (W) for the top 6 winners of primary metric (fast constraints)						
Benchmark	NTUgs	UFRGS-BRAZIL	PowerValve	Goldilocks	eOPT	CUsizer
b19_fast	2.71E+00	X	4.49E+00	1.78E+00	1.89E+00	X
des_perf_fast	2.39E+00	3.52E+00	2.32E+00	9.81E+00	5.87E+00	2.43E+00
DMA_fast	5.11E-01	3.23E-01	3.12E-01	6.87E-01	8.58E-01	4.89E-01
leon3mp_fast	X	X	4.94E+00	2.02E+00	2.42E+00	2.08E+00
netcard_fast	2.01E+00	2.30E+00	2.97E+00	2.06E+00	2.84E+00	2.46E+00
pci_bridge32_fast	5.12E-01	1.68E-01	2.26E-01	9.47E-01	4.08E-01	3.40E-01
vga_lcd_fast	7.58E-01	5.80E-01	7.73E-01	X	7.67E-01	8.60E-01

* “X” denotes the team fails to complete the benchmark with zero violation

Leakage for the Top 6 Winners of Primary Metric

Leakage data (W) for the top 6 winners of primary metric (slow constraints)						
Benchmark	NTUgs	UFRGS-BRAZIL	PowerValve	Goldilocks	eOPT	CUsizer
b19_slow	6.27E-01	6.14E-01	7.36E-01	7.58E-01	8.62E-01	5.02E+00
des_perf_slow	6.74E-01	8.84E-01	6.97E-01	9.47E-01	2.28E+00	1.13E+00
DMA_slow	2.05E-01	1.58E-01	1.47E-01	2.15E-01	4.51E-01	3.68E-01
leon3mp_slow	1.42E+00	1.79E+00	2.96E+00	1.47E+00	1.88E+00	1.92E+00
netcard_slow	1.77E+00	1.97E+00	1.94E+00	1.81E+00	2.10E+00	2.00E+00
pci_bridge32_slow	2.03E-01	1.15E-01	1.16E-01	6.96E-01	2.26E-01	2.88E-01
vga_lcd_slow	4.15E-01	3.78E-01	3.91E-01	4.63E-01	6.44E-01	7.53E-01

Run Time for the Top 6 Winners of Primary Metric

Run time (hr) for the top 6 winners of primary metric (fast constraints)						
Benchmark	NTUgs	UFRGS-BRAZIL	PowerValve	Goldilocks	eOPT	CUsizer
b19_fast	11.00	X	9.93	0.27	0.30	X
des_perf_fast	7.00	7.53	7.22	0.38	0.16	6.88
DMA_fast	1.72	0.54	1.52	0.04	0.03	0.59
leon3mp_fast	X	X	20.76	1.30	0.81	20.22
netcard_fast	29.00	31.36	28.89	3.61	1.20	18.17
pci_bridge32_fast	1.79	0.35	0.98	0.10	0.04	0.61
vga_lcd_fast	9.00	5.36	8.12	X	0.20	2.94

* “X” denotes the team fails to complete the benchmark with zero violation

Run Time for the Top 6 Winners of Primary Metric

Run time (hr) for the top 6 winners of primary metric (slow constraints)						
Benchmark	NTUgs	UFRGS-BRAZIL	PowerValve	Goldilocks	eOPT	CUsizer
b19_slow	11.00	8.29	9.93	0.44	0.29	5.02
des_perf_slow	7.00	7.25	7.22	0.29	0.15	1.13
DMA_slow	2.16	0.33	1.20	0.05	0.03	0.37
leon3mp_slow	20.00	22.54	20.76	1.56	0.80	1.92
netcard_slow	29.00	18.89	28.89	2.20	1.15	2.00
pci_bridge32_slow	2.26	0.27	0.91	0.05	0.04	0.29
vga_lcd_slow	9.00	3.70	8.12	0.22	0.19	0.75

Top 6 Quality Solution for Each Benchmark

DMA_fast		
Rank	Team	Leakage (W)
1	PowerValve	3.12E-01
2	UFRGS-BRAZIL	3.23E-01
3	CUsizer	4.89E-01
4	NTUgs	5.11E-01
5	Goldilocks	6.87E-01
6	SensOpt	7.40E-01

DMA_slow		
Rank	Team	Leakage (W)
1	PowerValve	1.47E-01
2	UFRGS-BRAZIL	1.58E-01
3	NTUgs	2.05E-01
4	SensOpt	2.13E-01
5	Goldilocks	2.15E-01
6	HBLR	3.15E-01

*** The affiliation/members for each team can be found at the contest website.**

Top 6 Quality Solution for Each Benchmark

b19_fast		
Rank	Team	Leakage (W)
1	NuTuner	1.04E+00
2	SensOpt	1.18E+00
3	Gatekeeper	1.47E+00
4	Goldilocks	1.78E+00
5	eOPT	1.89E+00
6	UIC Dart Lab	2.33E+00

b19_slow		
Rank	Team	Leakage (W)
1	UFRGS-BRAZIL	6.14E-01
2	NTUgs	6.27E-01
3	SensOpt	7.27E-01
4	PowerValve	7.36E-01
5	Goldilocks	7.58E-01
6	eOPT	8.62E-01

*** The affiliation/members for each team can be found at the contest website.**

Top 6 Quality Solution for Each Benchmark

des_perf_fast		
Rank	Team	Leakage (W)
1	PowerValve	2.32E+00
2	NTUgs	2.39E+00
3	CUsizer	2.43E+00
4	UFRGS-BRAZIL	3.52E+00
5	HBLR	5.27E+00
6	National Chung Cheng University	5.45E+00

des_perf_slow		
Rank	Team	Leakage (W)
1	NTUgs	6.74E-01
2	PowerValve	6.97E-01
3	UFRGS-BRAZIL	8.84E-01
4	Goldilocks	9.47E-01
5	CUsizer	1.13E+00
6	HBLR	1.35E+00

*** The affiliation/members for each team can be found at the contest website.**

Top 6 Quality Solution for Each Benchmark

leon3mp_fast		
Rank	Team	Leakage (W)
1	Goldilocks	2.02E+00
2	UIC Dart Lab	2.05E+00
3	CUsizer	2.08E+00
4	eOPT	2.42E+00
5	National Chung Cheng University	3.51E+00
6	PowerValve	4.94E+00

leon3mp_slow		
Rank	Team	Leakage (W)
1	NTUgs	1.42E+00
2	Goldilocks	1.47E+00
3	HBLR	1.59E+00
4	UIC Dart Lab	1.76E+00
5	UFRGS-BRAZIL	1.79E+00
6	eOPT	1.88E+00

*** The affiliation/members for each team can be found at the contest website.**

Top 6 Quality Solution for Each Benchmark

netcard_fast		
Rank	Team	Leakage (W)
1	NTUgs	2.01E+00
2	Goldilocks	2.06E+00
3	UFRGS-BRAZIL	2.30E+00
4	UIC Dart Lab	2.45E+00
5	CUsizer	2.46E+00
6	eOPT	2.84E+00

netcard_slow		
Rank	Team	Leakage (W)
1	NTUgs	1.77E+00
2	HBLR	1.80E+00
3	Goldilocks	1.81E+00
4	PowerValve	1.94E+00
5	UFRGS-BRAZIL	1.97E+00
6	CUsizer	2.00E+00

*** The affiliation/members for each team can be found at the contest website.**

Top 6 Quality Solution for Each Benchmark

pci_bridge_fast		
Rank	Team	Leakage (W)
1	UFRGS-BRAZIL	1.68E-01
2	PowerValve	2.26E-01
3	NuTuner	2.48E-01
4	CUsizer	3.40E-01
5	eOPT	4.08E-01
6	NTUgs	5.12E-01

pci_bridge_slow		
Rank	Team	Leakage (W)
1	UFRGS-BRAZIL	1.15E-01
2	PowerValve	1.16E-01
3	NuTuner	1.28E-01
4	NTUgs	2.03E-01
5	SensOpt	2.11E-01
6	eOPT	2.26E-01

*** The affiliation/members for each team can be found at the contest website.**

Top 6 Quality Solution for Each Benchmark

vga_lcd_fast		
Rank	Team	Leakage (W)
1	UFRGS-BRAZIL	5.80E-01
2	UIC Dart Lab	7.24E-01
3	NTUgs	7.58E-01
4	eOPT	7.67E-01
5	PowerValve	7.73E-01
6	CUsizer	8.60E-01

vga_lcd_slow		
Rank	Team	Leakage (W)
1	UFRGS-BRAZIL	3.78E-01
2	PowerValve	3.91E-01
3	NuTuner	4.10E-01
4	NTUgs	4.15E-01
5	Goldilocks	4.63E-01
6	UIC Dart Lab	5.08E-01

*** The affiliation/members for each team can be found at the contest website.**