ISPD 2012 Library Release Notes

Last modified: January 5, 2012

Disclaimer

- The information published in this presentation is subject to change.
- It is the contestants responsibility to check the website frequently to check for any updates until the submission deadline.

- **The library details in this document are given for your information only.**
  - **You do not have to understand all the details here.**
  - **You can simply use the values provided in the library (see the document titled "Contest details" on the contest website for library usage)**

Changes from Initial Library

- The cell list is the same; area, leakage, input cap, timing, etc. values have been updated.
- The area field is now no longer a duplicate of the leakage field. Be sure to use leakage instead of area to compute the power metric.
- The ratio of device sizes between the “n” and “p” parts of NAND and NOR gates has changed.
  - Previously, the device sizes of the parallel and series gates were identical, leading to significantly different pullup and pulldown delays.
  - Now, the internal device sizes have been chosen so the pullup and pulldown delays are similar, except for small power levels. (see foils 8 through 14 for exact size specs.)

Changes from Initial Library (cont.)

- The internal loading on the output pin of the NAND, NOR, and complex gates has been increased in an attempt to more accurately model the diffusion capacitance of these topologies. This slows the gates down with respect to an inverter.
- A simple current source model was used to determine the delay and slope tables. These tables are now different for delay and slope, and dependent on input slope and threshold voltage in a non-linear, but realistic manner. (See foil 18)

Cell Family List

in01	Inverter
na02	2-input NAND
na03	3-input NAND
na04	4-input NAND
no02	2-input NOR
in01	3-input NOR
no04	4-input NOR
ao12	AND-OR-INV !(a|(b&c))
ao22	AND-OR-INV !((a&b)|(c&d))
oa12	OR-AND-INV !(a&(b|c))
oa22	OR-AND-INV !((a|b)&(c|d))
ms00	Flip Flop

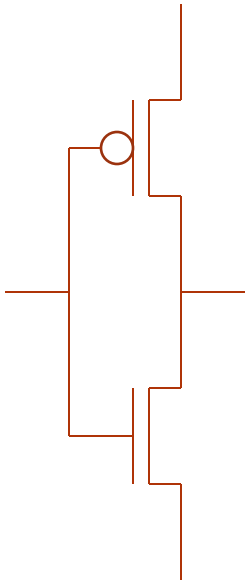
Device Sizes

	"01"			"02"			"03"			"04"			"06"			"08"			"10"			"20"			"40"			"80"		
	1			2			3			4			6			8			16			32			64			128		
	p sz	n sz	tot	p sz	n sz	tot	p sz	n sz	tot	p sz	n sz	tot	p sz	n sz	tot	p sz	n sz	tot	p sz	n sz	tot	p sz	n sz	tot	p sz	n sz	tot	p sz	n sz	tot
in01	1	1	2	2	2	4	3	3	6	4	4	8	6	6	12	8	8	16	16	16	32	32	32	64	64	64	128	128	128	256
na02	1	1	4	1	2	6	2	3	10	2	4	12	3	6	18	4	8	24	8	16	48	16	32	96	32	64	192	64	128	384
na03	1	1	6	1	2	9	1	3	12	2	4	18	2	6	24	3	8	33	6	16	66	11	32	129	22	64	258	43	128	513
na04	1	1	8	1	2	12	1	3	16	1	4	20	2	6	32	2	8	40	4	16	80	8	32	160	16	64	320	32	128	640
no02	1	1	4	2	1	6	3	2	10	4	2	12	6	3	18	8	4	24	16	8	48	32	16	96	64	32	192	128	64	384
no03	1	1	6	2	1	9	3	1	12	4	2	18	6	2	24	8	3	33	16	6	66	32	11	129	64	22	258	128	43	513
no04	1	1	8	2	1	12	3	1	16	4	1	20	6	2	32	8	2	40	16	4	80	32	8	160	64	16	320	128	32	640
ao12	1	1	6	2	2	12	3	3	18	4	4	24	6	6	36	8	8	48	16	16	96	32	32	192	64	64	384	128	128	768
ao22	1	1	8	2	2	16	3	3	24	4	4	32	6	6	48	8	8	64	16	16	128	32	32	256	64	64	512	128	128	1024
oa12	1	1	6	2	2	12	3	3	18	4	4	24	6	6	36	8	8	48	16	16	96	32	32	192	64	64	384	128	128	768
oa22	1	1	8	2	2	16	3	3	24	4	4	32	6	6	48	8	8	64	16	16	128	32	32	256	64	64	512	128	128	1024

Each cell comes in three variants: “s”, “m”, and “f” corresponding to different threshold voltages.

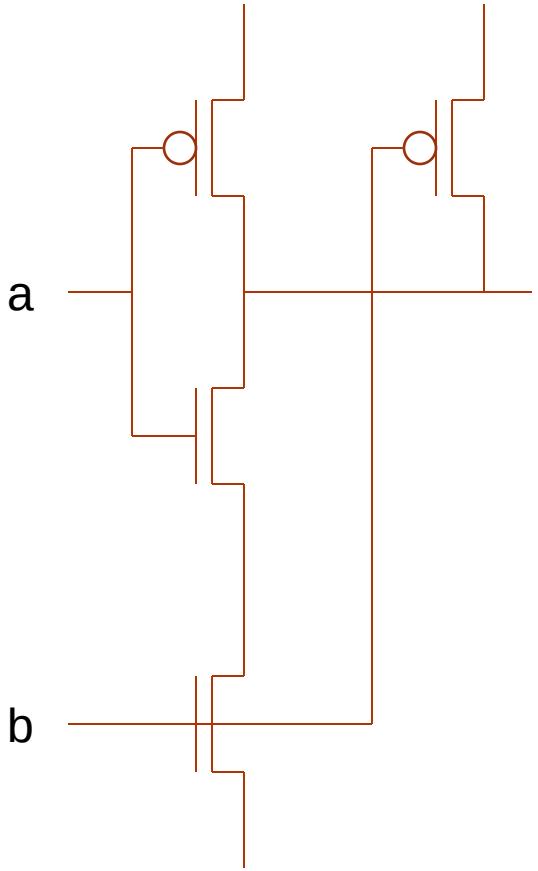
The “s” cells are slower, but have lower leakage power than the “m” or “f” cells. The “m” cells are slower than the “f” cells, but faster than the “s” cells, with corresponding differences in leakage power.

“in01” Inverter



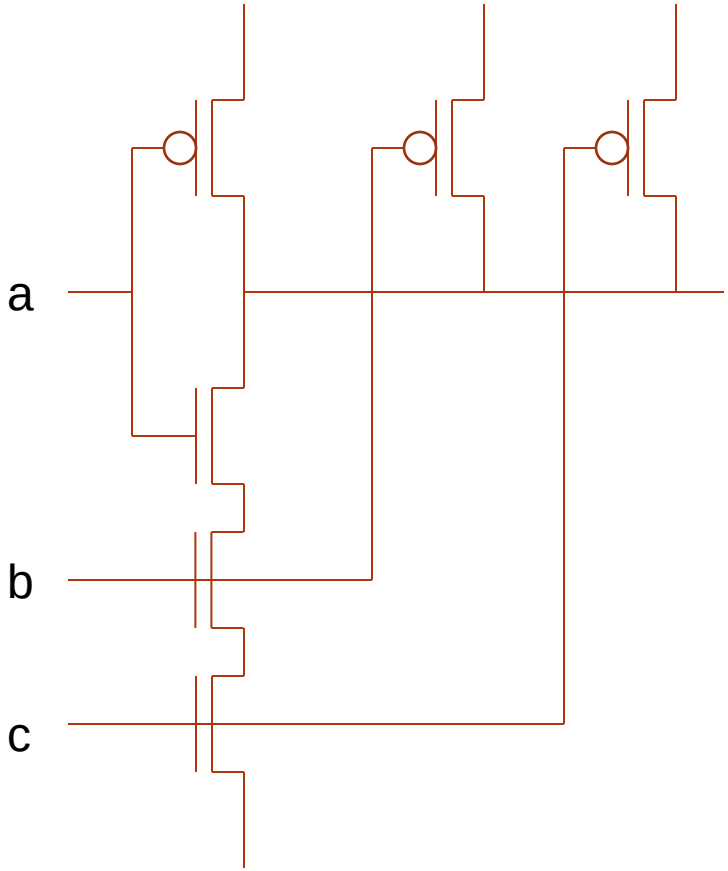
	"01"			"02"			"03"			"04"			"06"			"08"			"10"			"20"			"40"			"80"		
	1			2			3			4			6			8			16			32			64			128		
	p sz	n sz	tot	p sz	n sz	tot	p sz	n sz	tot	p sz	n sz	tot	p sz	n sz	tot	p sz	n sz	tot	p sz	n sz	tot	p sz	n sz	tot	p sz	n sz	tot	p sz	n sz	tot
in01	1	1	2	2	2	4	3	3	6	4	4	8	6	6	12	8	8	16	16	16	32	32	32	64	64	64	128	128	128	256

“na02” 2-input NAND



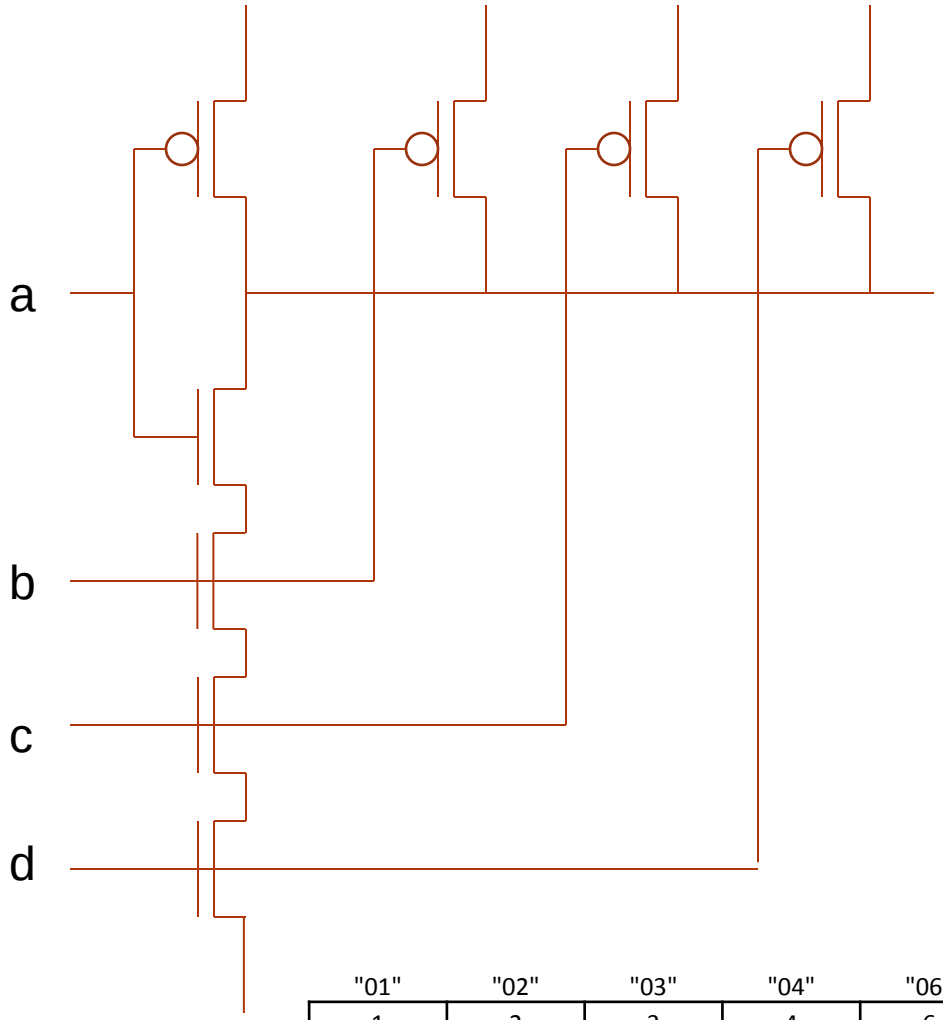
	"01"			"02"			"03"			"04"			"06"			"08"			"10"			"20"			"40"			"80"		
	1			2			3			4			6			8			16			32			64			128		
	p sz	n sz	tot	p sz	n sz	tot	p sz	n sz	tot	p sz	n sz	tot	p sz	n sz	tot	p sz	n sz	tot	p sz	n sz	tot	p sz	n sz	tot	p sz	n sz	tot	p sz	n sz	tot
na02	1	1	4	1	2	6	2	3	10	2	4	12	3	6	18	4	8	24	8	16	48	16	32	96	32	64	192	64	128	384

“na03” 3-input NAND



	"01"			"02"			"03"			"04"			"06"			"08"			"10"			"20"			"40"			"80"		
	1			2			3			4			6			8			16			32			64			128		
	p sz	n sz	tot	p sz	n sz	tot	p sz	n sz	tot	p sz	n sz	tot	p sz	n sz	tot	p sz	n sz	tot	p sz	n sz	tot	p sz	n sz	tot	p sz	n sz	tot	p sz	n sz	tot
na03	1	1	6	1	2	9	1	3	12	2	4	18	2	6	24	3	8	33	6	16	66	11	32	129	22	64	258	43	128	513

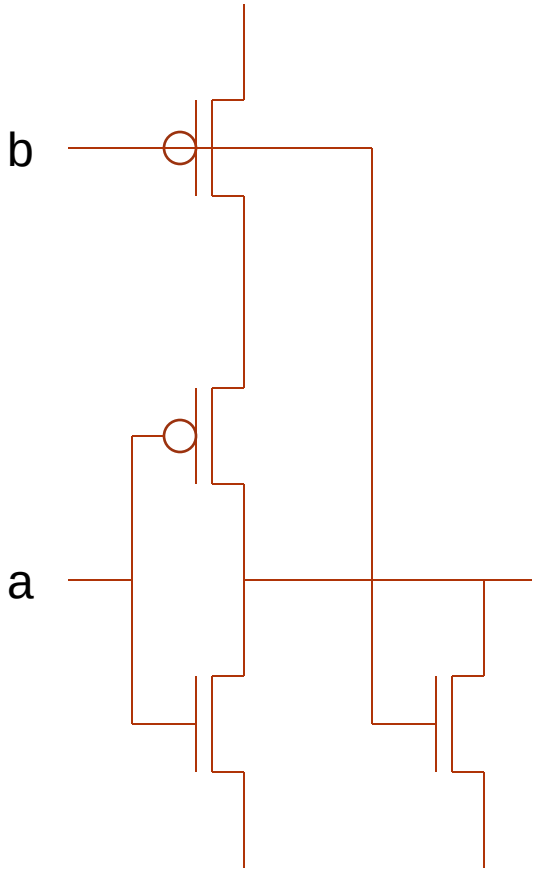
“na04” 4-input NAND



"01"			"02"			"03"			"04"			"06"			"08"			"10"			"20"			"40"			"80"		
1			2			3			4			6			8			16			32			64			128		
p sz	n sz	tot	p sz	n sz	tot	p sz	n sz	tot	p sz	n sz	tot	p sz	n sz	tot	p sz	n sz	tot	p sz	n sz	tot	p sz	n sz	tot	p sz	n sz	tot	p sz	n sz	tot
1	1	8	1	2	12	1	3	16	1	4	20	2	6	32	2	8	40	4	16	80	8	32	160	16	64	320	32	128	640

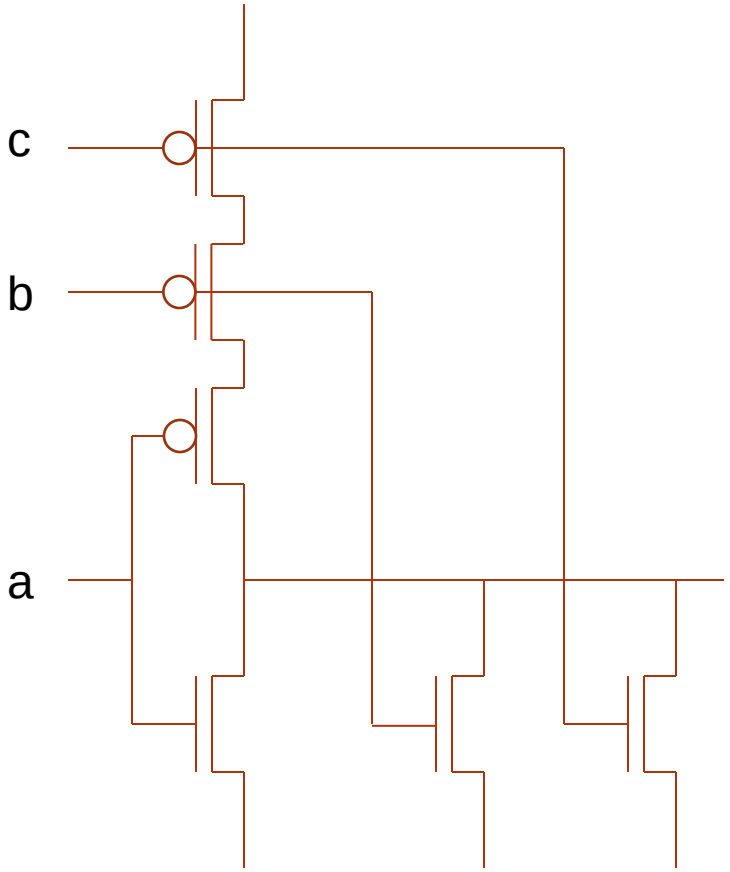
na04

“no02” 2-input NOR



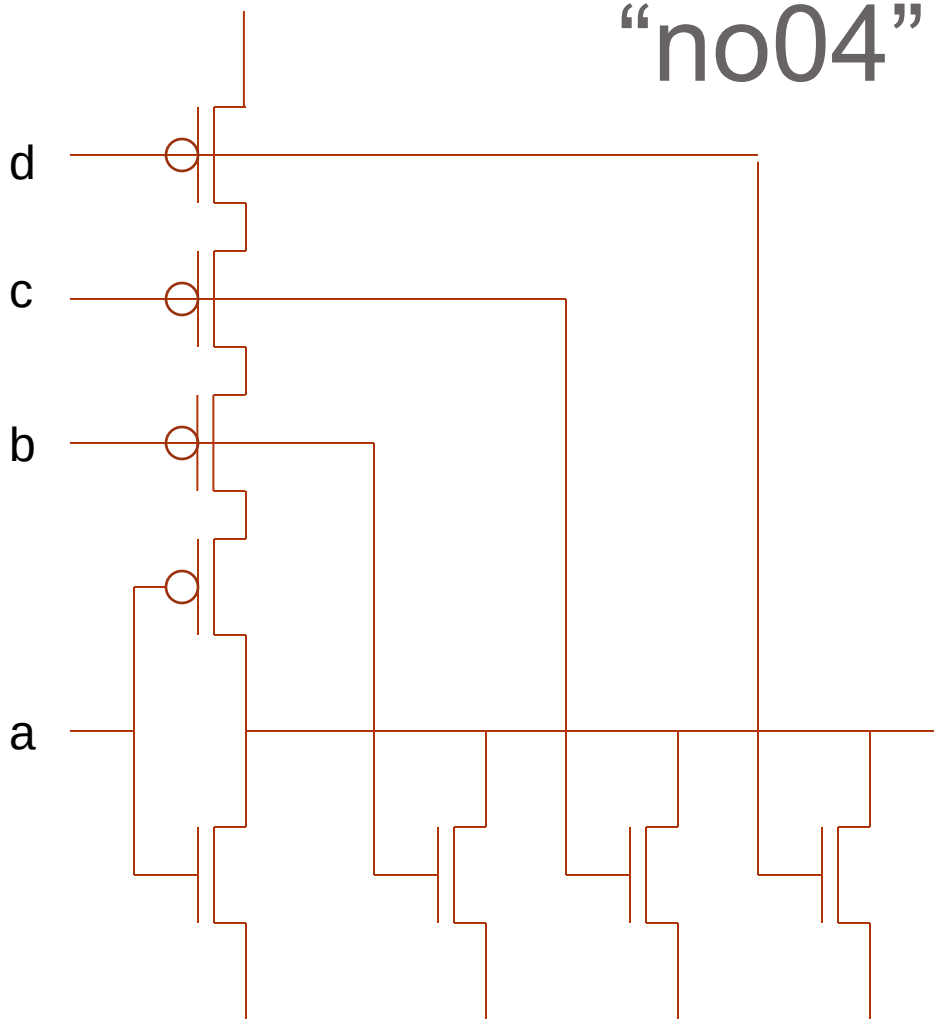
	"01"			"02"			"03"			"04"			"06"			"08"			"10"			"20"			"40"			"80"		
	1			2			3			4			6			8			16			32			64			128		
	p sz	n sz	tot	p sz	n sz	tot	p sz	n sz	tot	p sz	n sz	tot	p sz	n sz	tot	p sz	n sz	tot	p sz	n sz	tot	p sz	n sz	tot	p sz	n sz	tot	p sz	n sz	tot
no02	1	1	4	2	1	6	3	2	10	4	2	12	6	3	18	8	4	24	16	8	48	32	16	96	64	32	192	128	64	384

“no03” 3-input NOR



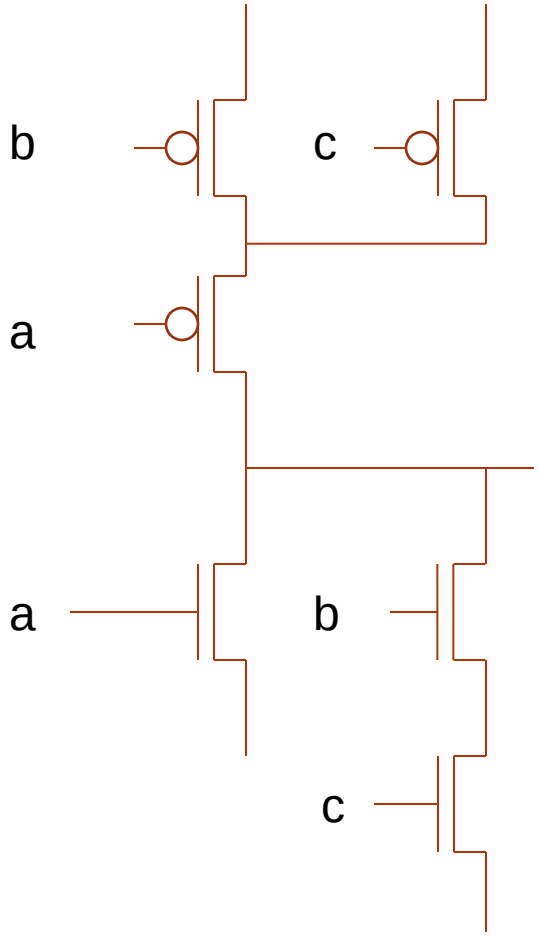
	"01"			"02"			"03"			"04"			"06"			"08"			"10"			"20"			"40"			"80"		
	1			2			3			4			6			8			16			32			64			128		
	p sz	n sz	tot	p sz	n sz	tot	p sz	n sz	tot	p sz	n sz	tot	p sz	n sz	tot	p sz	n sz	tot	p sz	n sz	tot	p sz	n sz	tot	p sz	n sz	tot	p sz	n sz	tot
no03	1	1	6	2	1	9	3	1	12	4	2	18	6	2	24	8	3	33	16	6	66	32	11	129	64	22	258	128	43	513

“no04” 4-input NOR



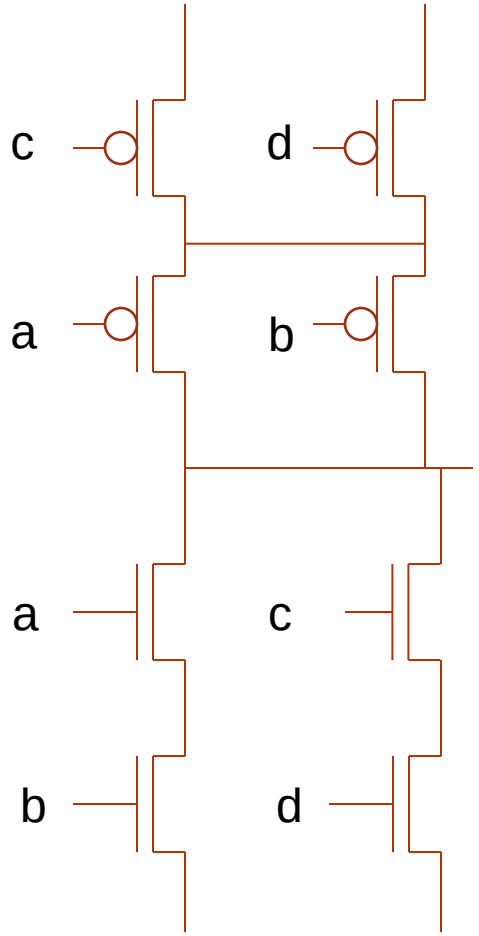
	"01"			"02"			"03"			"04"			"06"			"08"			"10"			"20"			"40"			"80"		
	1			2			3			4			6			8			16			32			64			128		
	p sz	n sz	tot	p sz	n sz	tot	p sz	n sz	tot	p sz	n sz	tot	p sz	n sz	tot	p sz	n sz	tot	p sz	n sz	tot	p sz	n sz	tot	p sz	n sz	tot	p sz	n sz	tot
no04	1	1	8	2	1	12	3	1	16	4	1	20	6	2	32	8	2	40	16	4	80	32	8	160	64	16	320	128	32	640

“ao12” And-Or-Inv



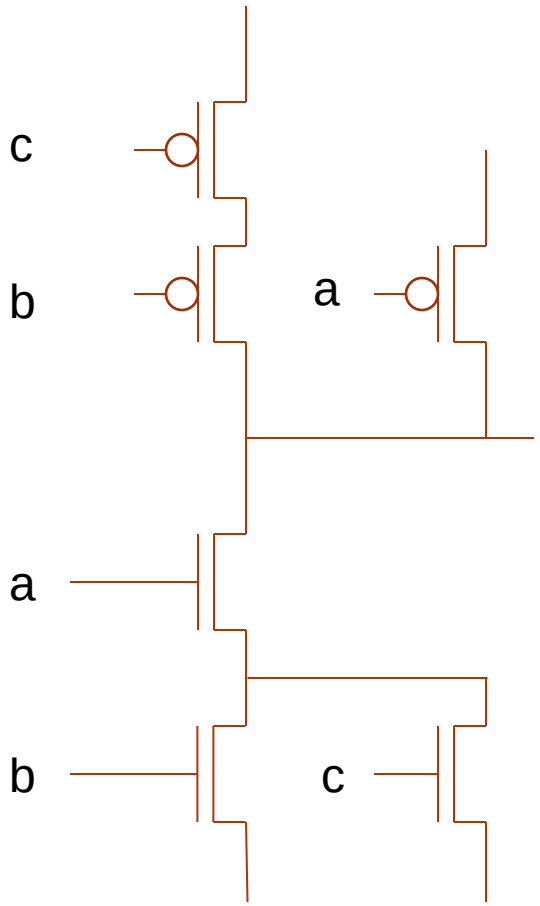
	"01"			"02"			"03"			"04"			"06"			"08"			"10"			"20"			"40"			"80"		
	1			2			3			4			6			8			16			32			64			128		
	p sz	n sz	tot	p sz	n sz	tot	p sz	n sz	tot	p sz	n sz	tot	p sz	n sz	tot	p sz	n sz	tot	p sz	n sz	tot	p sz	n sz	tot	p sz	n sz	tot	p sz	n sz	tot
ao12	1	1	6	2	2	12	3	3	18	4	4	24	6	6	36	8	8	48	16	16	96	32	32	192	64	64	384	128	128	768

“ao22” And-Or-Inv



	"01"			"02"			"03"			"04"			"06"			"08"			"10"			"20"			"40"			"80"		
	1			2			3			4			6			8			16			32			64			128		
	p sz	n sz	tot	p sz	n sz	tot	p sz	n sz	tot	p sz	n sz	tot	p sz	n sz	tot	p sz	n sz	tot	p sz	n sz	tot	p sz	n sz	tot	p sz	n sz	tot	p sz	n sz	tot
ao22	1	1	8	2	2	16	3	3	24	4	4	32	6	6	48	8	8	64	16	16	128	32	32	256	64	64	512	128	128	1024

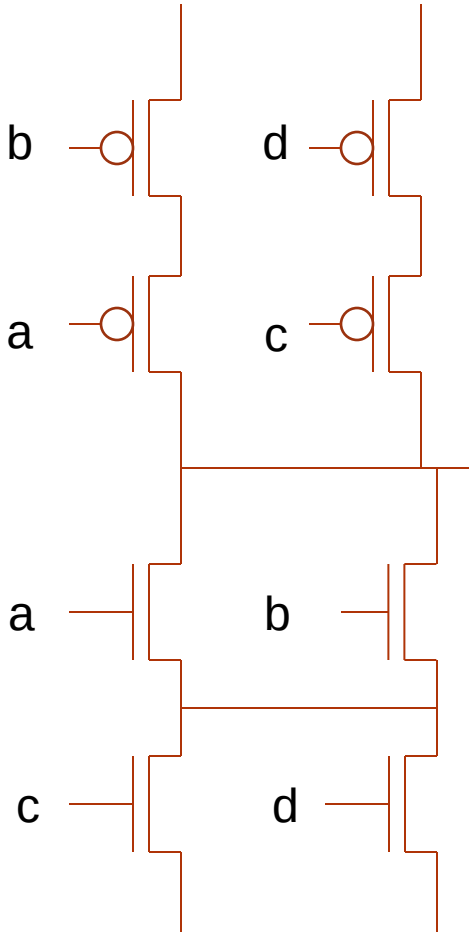
“oa12” And-Or-Inv



"01"			"02"			"03"			"04"			"06"			"08"			"10"			"20"			"40"			"80"		
1			2			3			4			6			8			16			32			64			128		
p sz	n sz	tot	p sz	n sz	tot	p sz	n sz	tot	p sz	n sz	tot	p sz	n sz	tot	p sz	n sz	tot	p sz	n sz	tot	p sz	n sz	tot	p sz	n sz	tot	p sz	n sz	tot
1	1	6	2	2	12	3	3	18	4	4	24	6	6	36	8	8	48	16	16	96	32	32	192	64	64	384	128	128	768

oa12

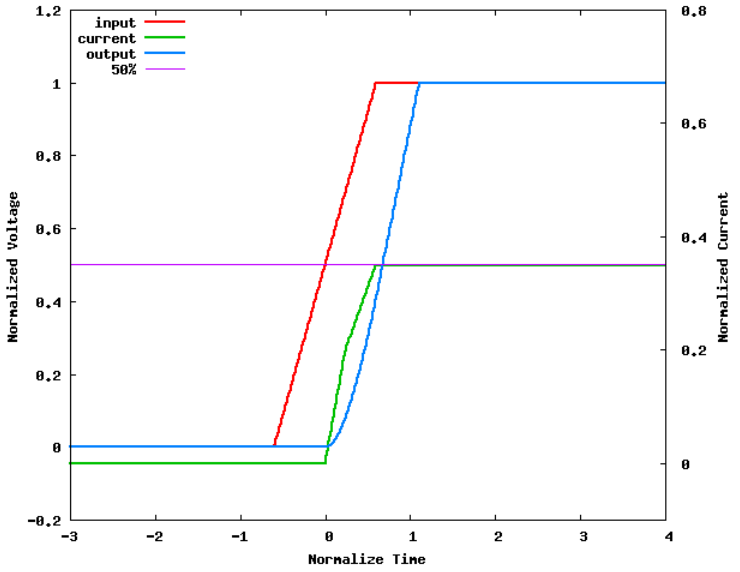
“oa22” And-Or-Inv

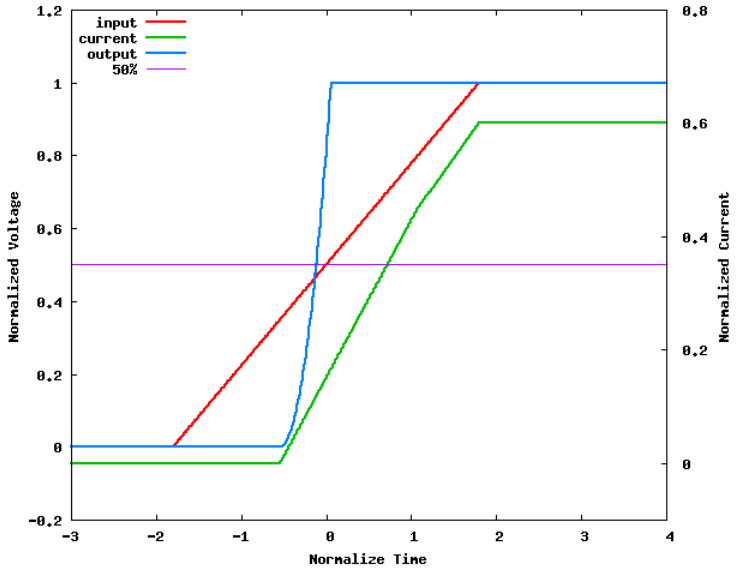


	"01"			"02"			"03"			"04"			"06"			"08"			"10"			"20"			"40"			"80"		
	1			2			3			4			6			8			16			32			64			128		
	p sz	n sz	tot	p sz	n sz	tot	p sz	n sz	tot	p sz	n sz	tot	p sz	n sz	tot	p sz	n sz	tot	p sz	n sz	tot	p sz	n sz	tot	p sz	n sz	tot	p sz	n sz	tot
oa22	1	1	8	2	2	16	3	3	24	4	4	32	6	6	48	8	8	64	16	16	128	32	32	256	64	64	512	128	128	1024

Delay/Slope Modeling

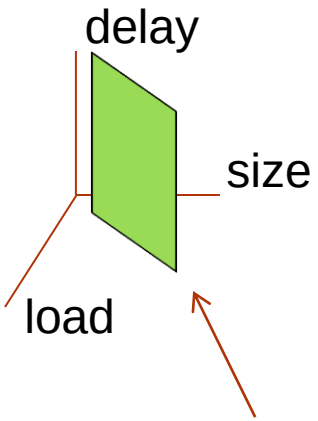
- We used a simple current source model to determine delays and slopes.
- The model comprehends: slope, threshold voltages, and ratio of driver size to opposing size.
- Delays could be negative as illustrated on the right. (No negative delays in the current tables.)





Characterization Curves

- Graphs show delay as a function of size with a constant ratio between load and size.
- There is relatively more internal loading on smaller cells due to legging effects.
- The equal delay size ratio for a NA03 cannot be satisfied for small sizes, leading to the non-monotonicities in the right plot.



Constant ratio between load and size