

ISPD 2010 - High Performance Clock Network Synthesis Contest and the Benchmark Suite

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Why Another Clock Contest?

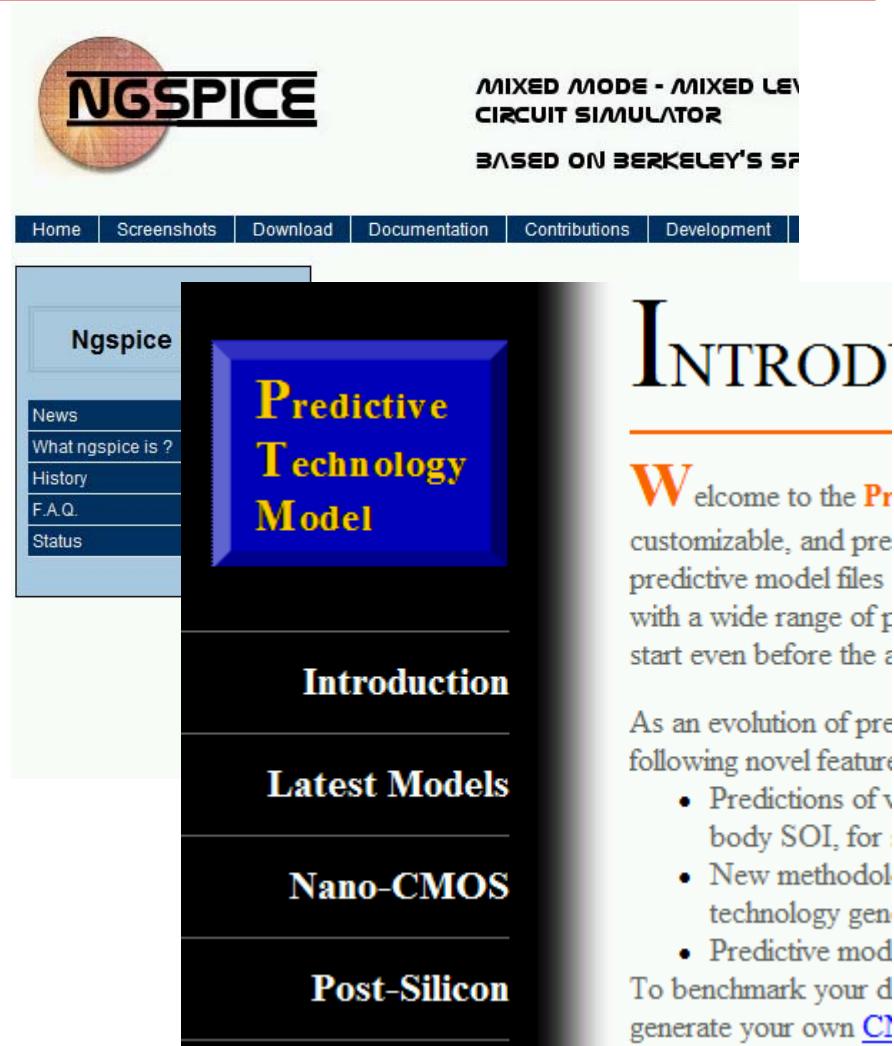
- ISPD Contests
 - Placement Contest 2005, 2006
 - Routing Contest 2007, 2008
 - Clock Synthesis Contest 2009, [2010](#)
- Just another Clock Contest?
 - No!
 - Major difference
 - Hundreds of simulations vs 2
 - Sub-10ps clock skew limit
 - Both Vdd and wire width variations
 - Real clock benchmarks from both IBM and Intel microprocessor designs
 - ~10x more clock sinks

Review of 2009 Clock Synthesis Contest

- Basic Formulation
 - Power limited
 - As total capacitance of inverter and wire
 - Real clock skew considering PVT variation (w/ SPICE)
 - 2 simulations in different Vdd
 - Clock Latency Range (CLR)
 - maximum difference of clock arrival time of any arbitrary pair of clock sinks from the 2 different Vdd simulations
 - upper bound of the actual skew
 - Non-tree is allowed
 - Bigger inverter can be formed by connecting multiple inverters in parallel (No limit)
 - No legalization is needed
 - Different wire size can be formed by connecting multiple wires in parallel
 - Wire is modeled as 2 end-points
 - Routing congestion not considered
 - No routing blockages

2009 CNS Contest Details

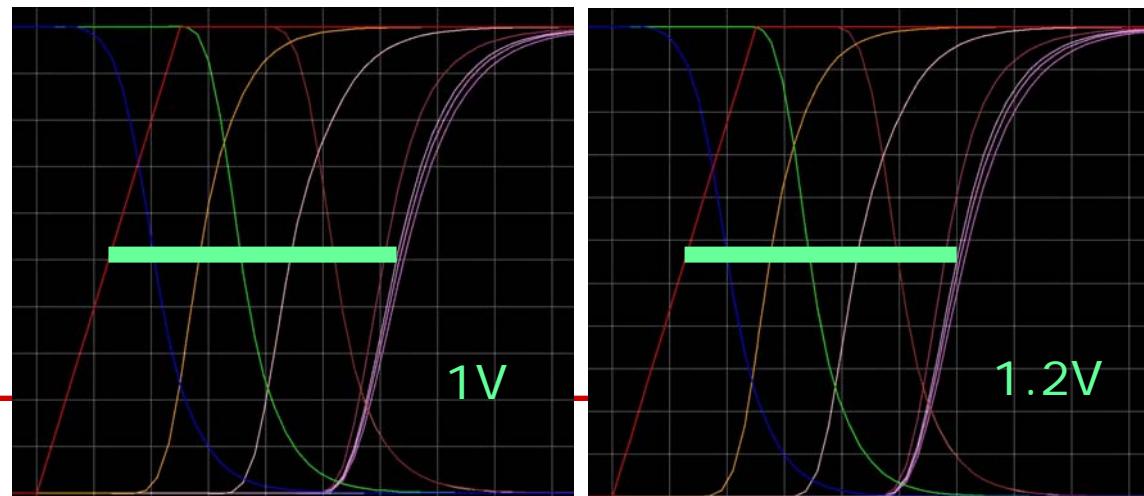
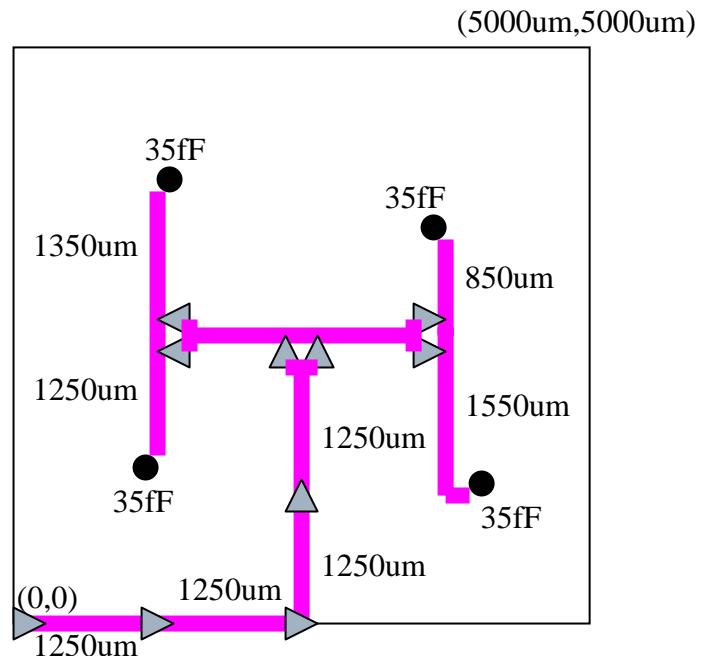
- Ngspice release 18
- Predictive Technology Model (PTM 45nm HP)
 - Matches IBM model for HP uP
- Two inverters
 - Mid-sized inverter
 - 10um nmos, 14.6um pmos (for similar R/F delay)
 - input cap = 35fF
resistance = 61.2Ohm
output parasitic cap = 80fF
 - Small inverter
 - 1.37um nmos, 2um pmos
 - input cap = 4.2fF,
resistance = 440Ohm,
output parasitic cap = 6.1fF



2009 CNS Contest Details (2)

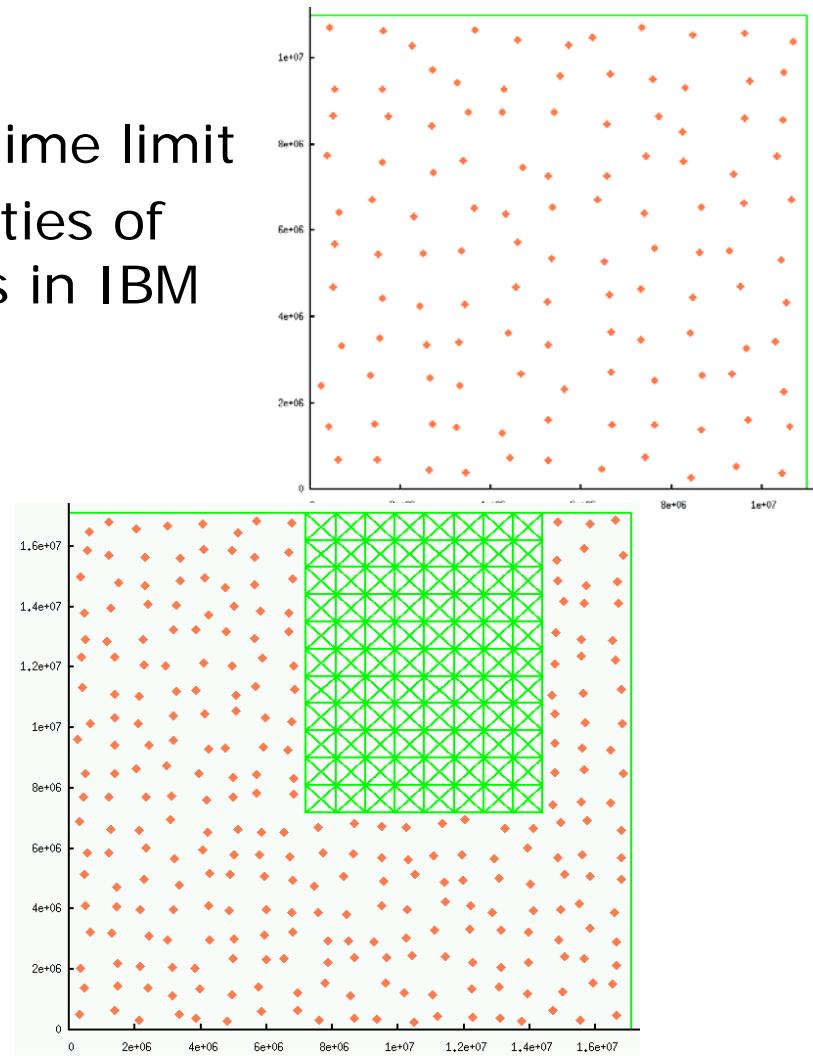
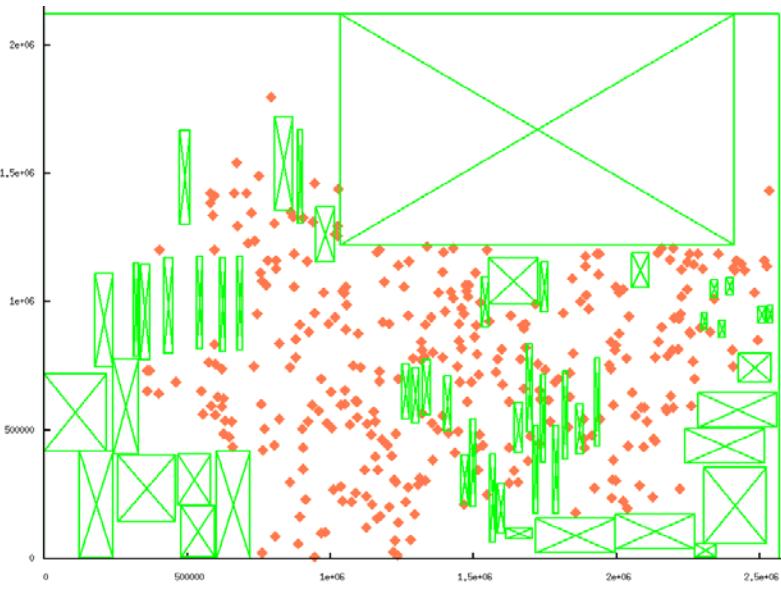
Inverters
connected
in parallel

- Two wire types
 - Loosely based on IBM 45nm technology data
 - Wide 0.1 Ohm/um 0.2 fF/um
 - Narrow 0.3 Ohm/um 0.16 fF/um
- Slew (10%-90%) limit = 100ps
- The source is directly driving the mid-sized inverter.
- The input slew to this inverter is 100ps.
- Clock source is at (0,0).
- Vdd = 1V
- Clock frequency = 2GHz
- Clock period = 500ps



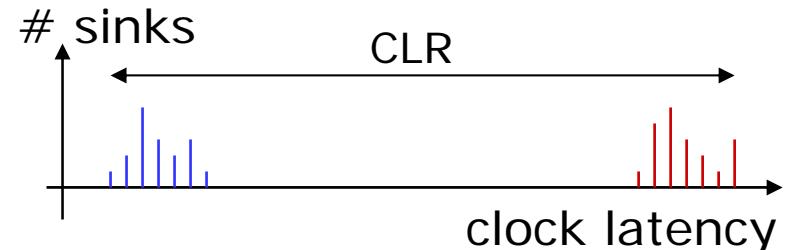
2009 CNS Contest Benchmarks

- 10 Benchmarks released
 - 7 used in contest due to time limit
- Roughly based on the properties of real clock synthesis problems in IBM
- Sink count : 91 - 330



Lessons Learned from Last year

- Clock latency range (CLR) is not practical
 - This upper bound is too loose
 - What if we use CLR for MCMM?
- No wire variation is considered
 - Encourage more wire delay
- Not challenging enough
 - Minimize CLR with power limit
 - All teams use clock trees
 - Best nominal skew: ~5ps
 - Best CLR: ~30ps
 - Skew requirement should be tighter
- The contest was a mixture of ASIC methodology and server methodology
 - ASIC needs very fast algorithm (clock tree)
 - 20k sinks for 5 mins (parallel programming?)
 - No SPICE, Elmore or moment matching
 - Microprocessor demands high robustness (grid)
 - Skew with OCV < 10ps
 - SPICE simulation with greatest accuracy
- Contest deadline was too close to ICCAD deadline



What's new for 2010?

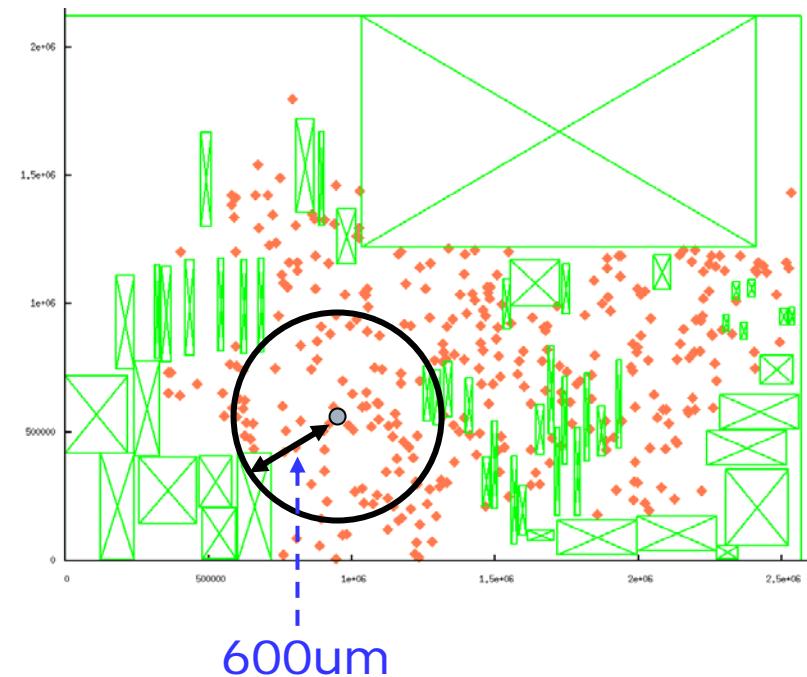
- A local clock skew limit
- To minimize total clock capacitance
- Much more clock sinks than 2009
 - From 981 to 2249 (compare to 91 - 330 in 2009)
 - New ngspice (version 20) is much faster
- Variations on inverter supply voltage and wire width
- Benchmarks from real IBM and Intel microprocessor designs

Voltage and wire width variations

- Power supply voltage of each inverter is a random variable
 - max +/- 7.5% variation
- Width of each wire segment is a random variable
 - Max +/- 5% variation
- Use PERL rand() to generate a random number for each random variables
 - Uniform distribution
- Other thought: we can use the MC engine in ngspice if it is ready

New objective for 2010 : Local Clock Skew

- Local Clock Skew (LCS)
 - Compute clock skew only for a pair of “local clock sinks”
 - Local clock sinks: distance less than “local skew distance”
 - 600um as an example
 - Ignore clock skew for far sinks
 - Wire snaking/buffer insertion to fix hold-time violation
- Generic
 - We can set local skew distance to infinite
- Practical
 - Being used in the industry
 - Multiple distance/skew requirements



Timeline

- 2009-APR : Comments! Comments!
 - 2009-JUL : Discussions! Discussions! Discussions!
 - 2009-OCT : Announcement of 2010 CNS contest
 - 2009-DEC-7 : Detailed rules posted in website with the release of the new evaluation script
 - 2009-DEC-8 : Registration deadline (20 initial teams)
 - 2010-JAN-10 : Alpha executable (17 teams left)
 - 2010-FEB-8 : Final executable submission (13 final teams)
 - 2010-FEB-10 : Test completed (10 finalists)

 - 2010-MAR-16 : Announcement of results
-

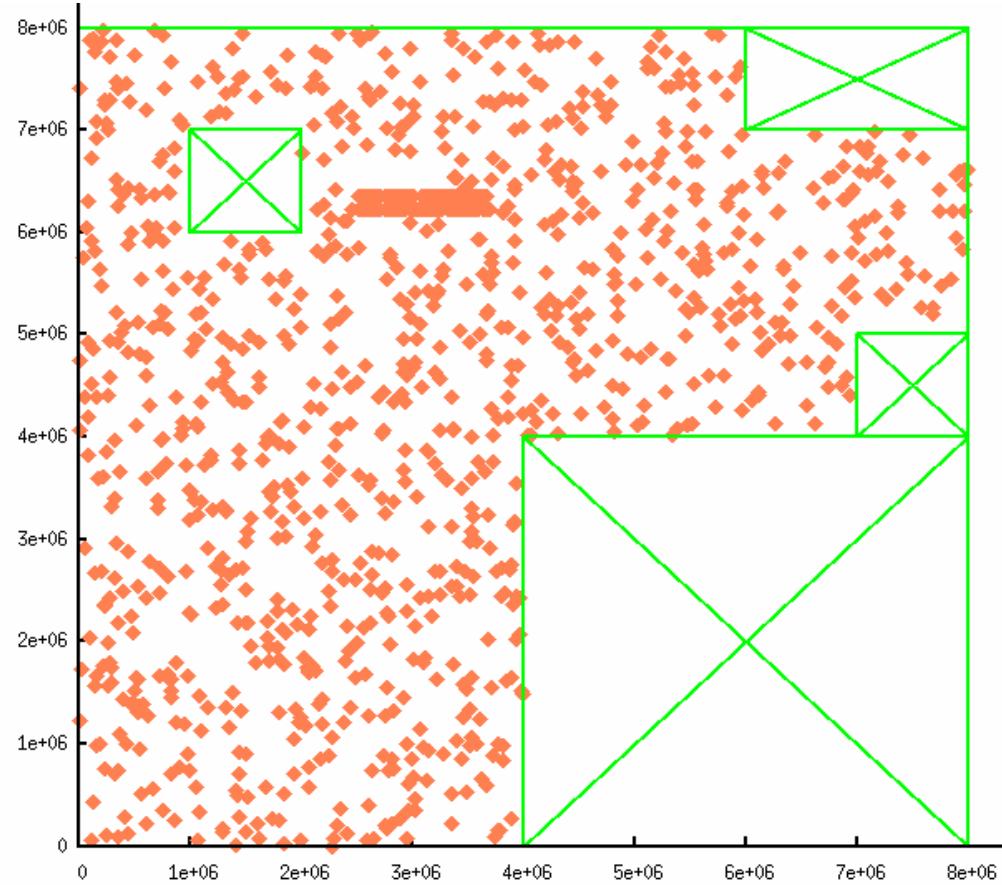
Our Teams

- 20 teams registered
 - 7 from North America
 - 1 from Europe
 - 12 from Asia
- 17 alpha executables
- 13 final teams
 - 6 from North America
- 10 teams passed final test

id	Affiliation	Contact Author
01	Polytechnic University of Hong Kong	Jingwei Lu
-	-	-
-	-	-
04	University of Illinois at Urbana-Champaign	Ying-Yu Chen
-	-	-
06	Tsinghua University	Feifei Niu
07	NCTU, CS, Taiwan	Wen-Hao Liu
08	National Taiwan University	Xin-Wei Shih
09	Chinese University of Hong Kong	Linfu Xiao
10	National Cheng Kung University, Taiwan	Sheng Chou
-	-	-
-	-	-
13	Chung Yuan Christian University, Taiwan	Jui-Hung Hung
-	-	-
15	University of Michigan	Dongjin Lee
16	UT Austin	Yilin Zhang
-	-	-
-	-	-
19	University of Calgary	Logan Rakai
20	Purdue University	Tarun Mittal
-	-	-
22	University of California at Santa Cruz	Xuchu Hu

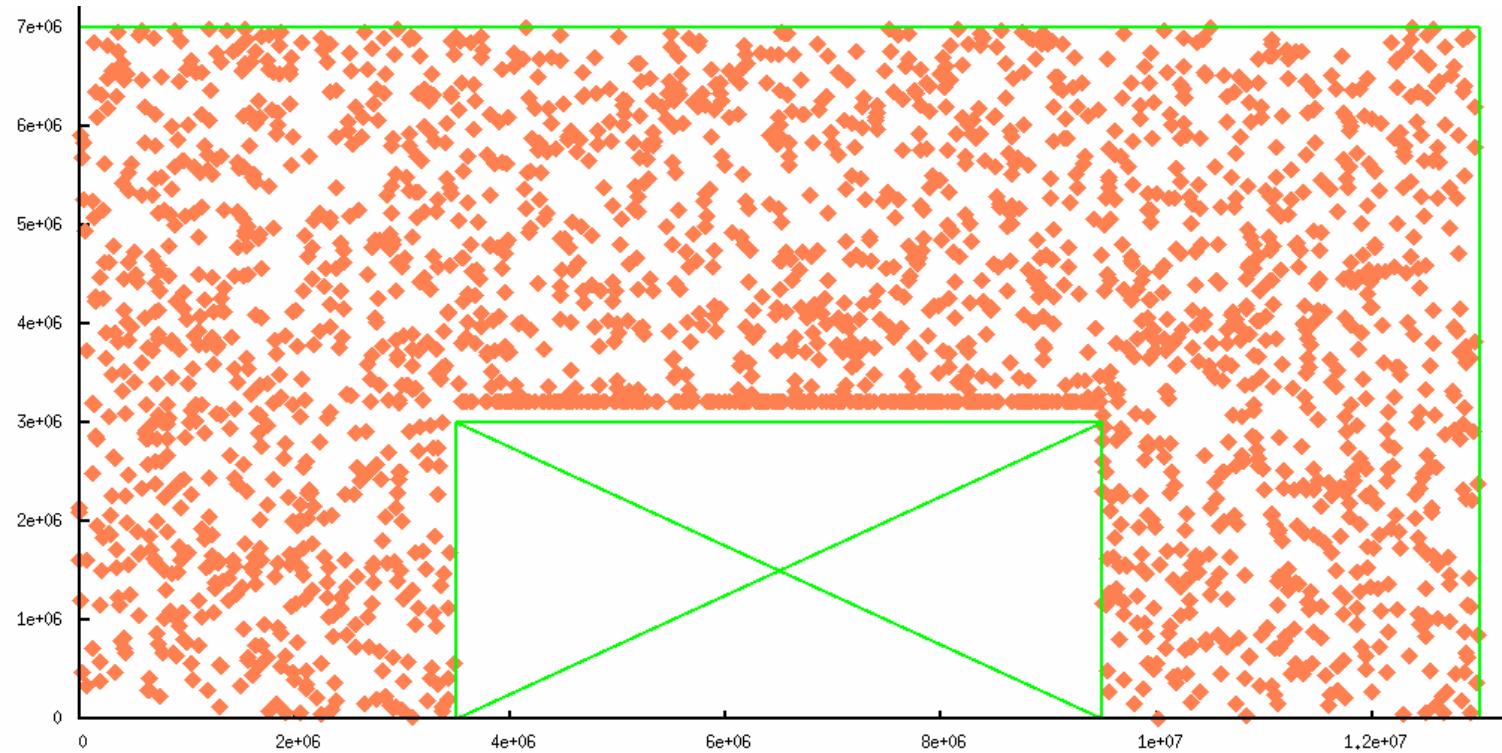
ispd10cns01

- Area: 64mm²
- # sinks: 1107
- Roughly based on real clock problems
- 4 blockages
- Local Skew Distance 600um
- Local Skew Limit 7.5ps



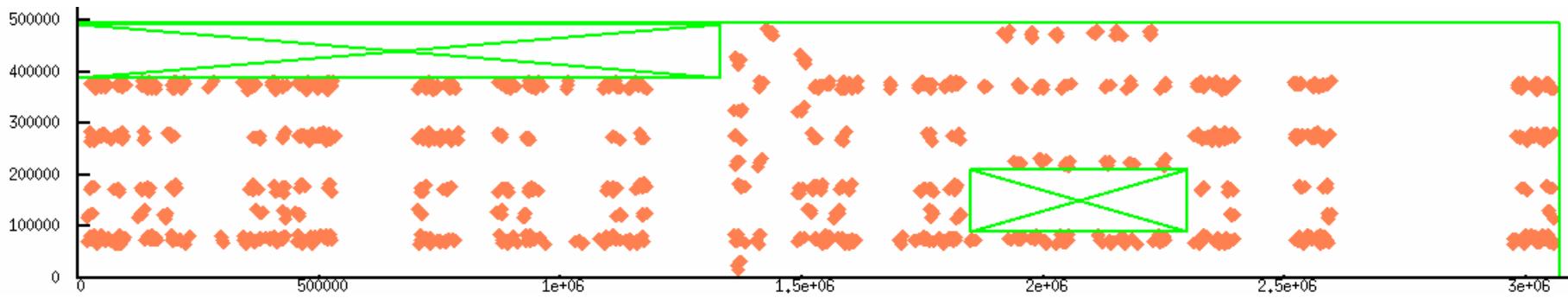
ispd10cns02

- Area: 91mm²
- # sinks: 2249 (largest in suite)
- Roughly based on real clock problems
- 1 big blockage at bottom
- Local Skew Distance 600um
- Local Skew Limit 7.5ps



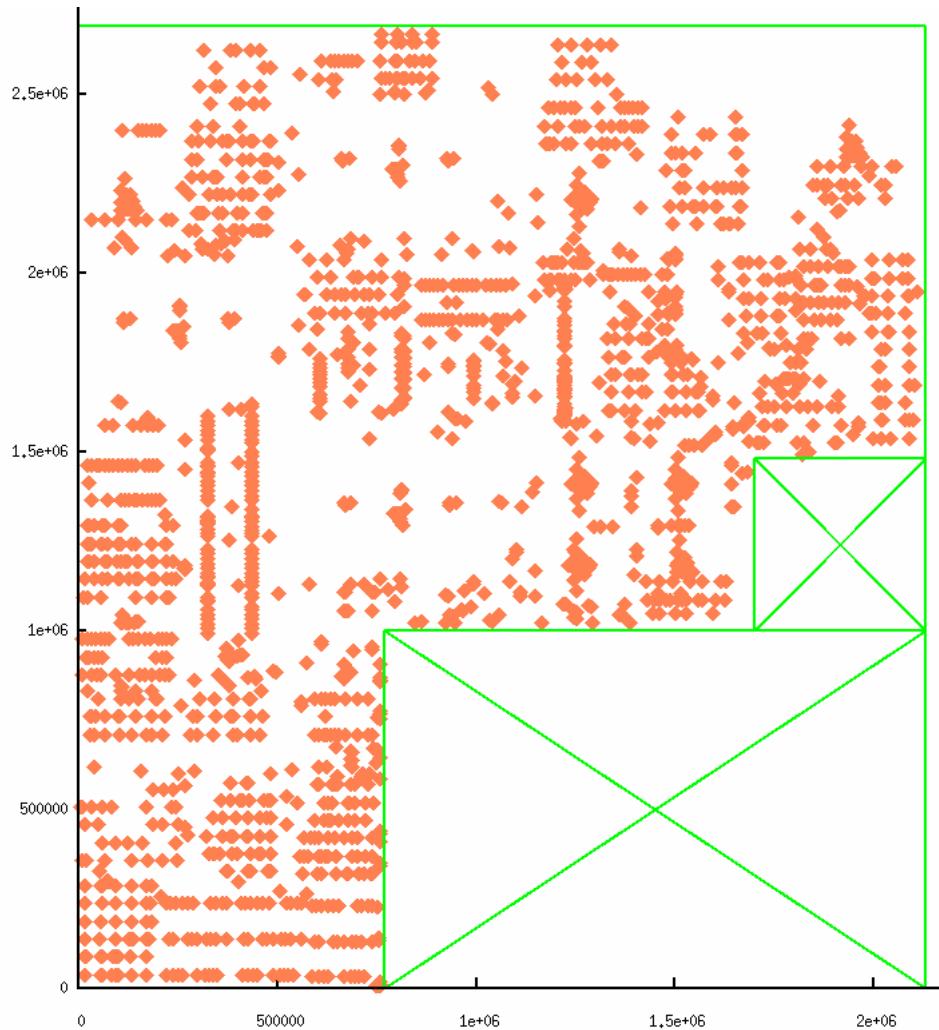
ispd10cns03

- Area: 1.5mm²
- Smallest in suite
- # sinks: 1200
- Based on real microprocessor designs, scaled to 45nm
- 2 blockages
- Local Skew Distance 370um
- Local Skew Limit 4.999ps



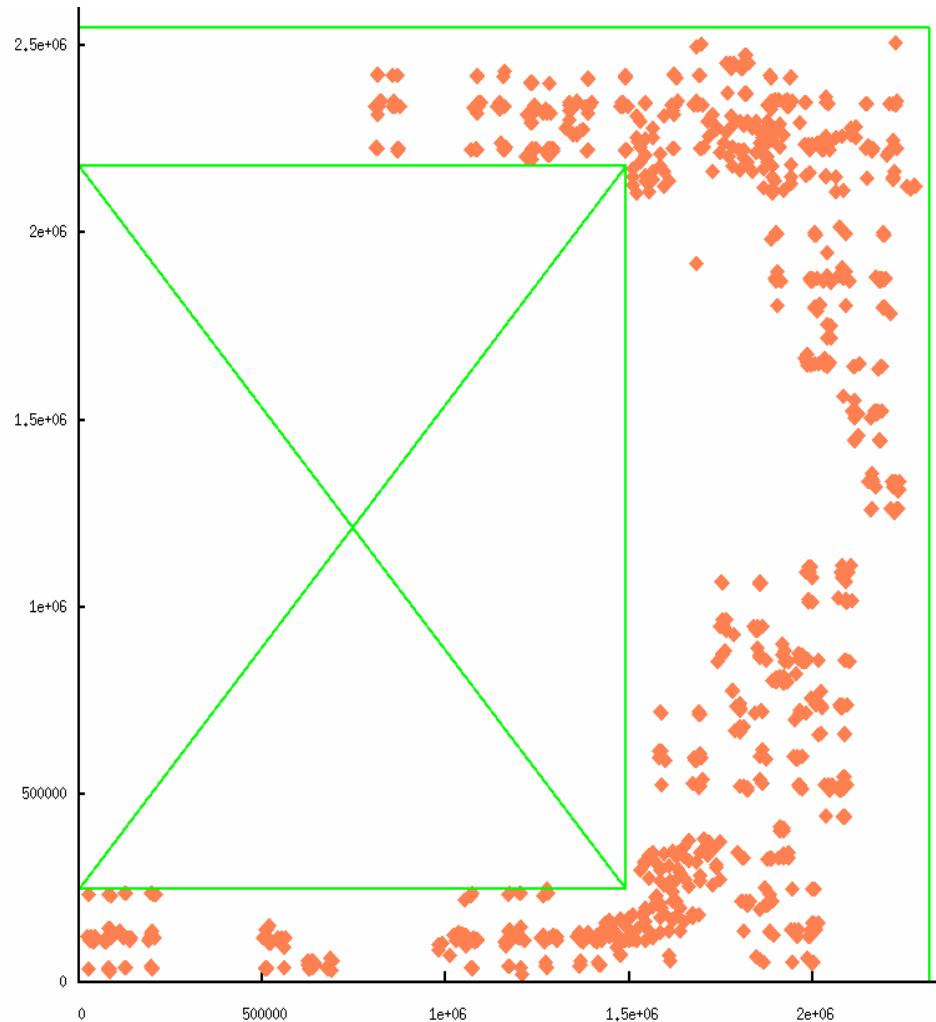
ispd10cns04

- Area: 5.7mm²
- # sinks: 1845
- Based on real microprocessor designs, scaled to 45nm
- 2 blockages at bottom right corner
- Local Skew Distance 600um
- Local Skew Limit 7.5ps



ispd10cns05

- Area: 5.9mm²
- # sinks: 1016
- Based on real microprocessor designs, scaled to 45nm
- huge blockage on the left
- Local Skew Distance 600um
- Local Skew Limit 7.5ps

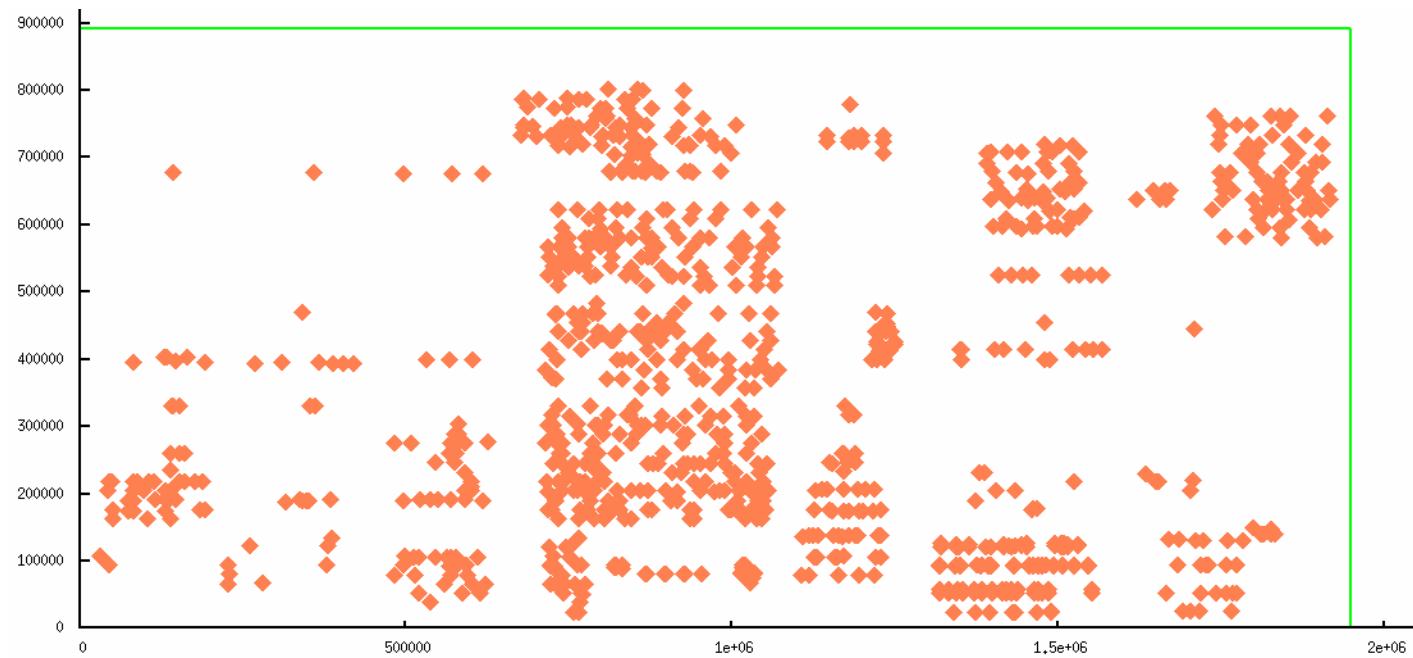


Benchmarks from Intel

- Special thanks to
 - Mustafa Ozdal, Rupesh Shelar, Steve Burns
- 11 benchmarks
 - No blockages
 - # of sinks : 140-1917
 - X in poly pitch (track)
 - Y in circuit row
 - Capacitance loading in minimum inverter input cap
- For this contest
 - Picked 3 with most # of sinks (986, 1917, 1137)
 - Scaling
 - 160nm pitch
 - A circuit row has 12 tracks
 - Min inverter - 0.5 um gate width (45nm) ~ 1.5fF
 - Remove all sinks at the same location

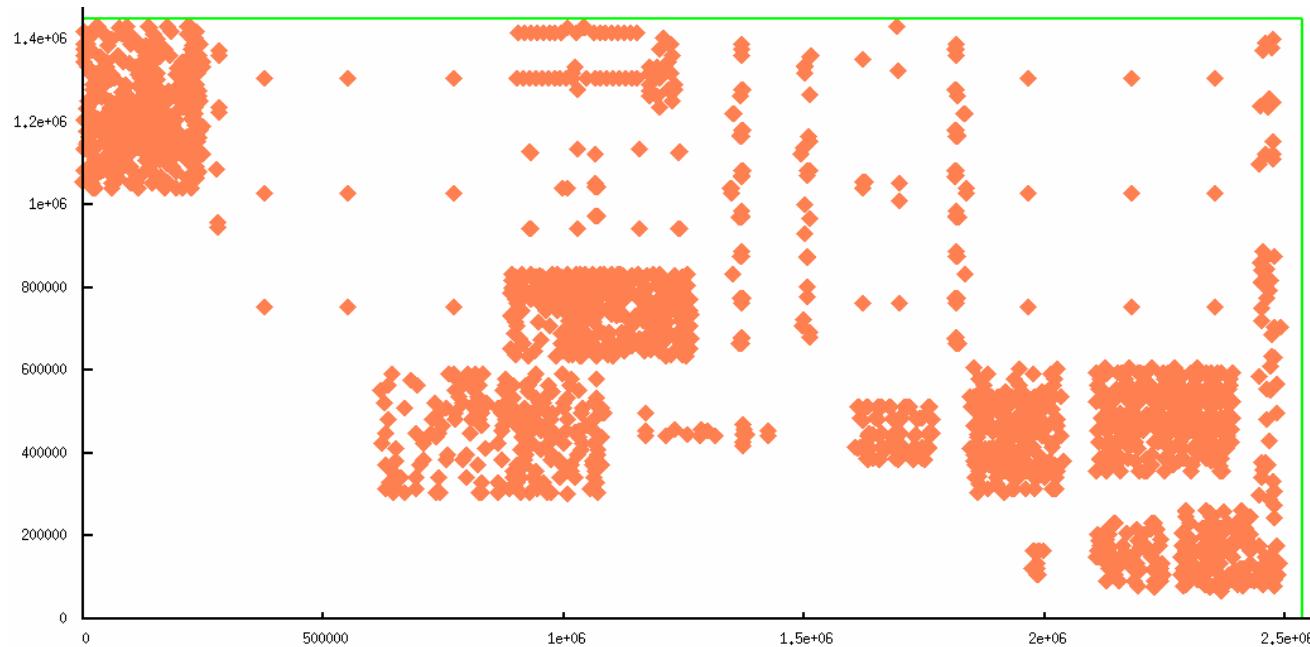
ispd10cns06

- Area: 1.7mm²
- # sinks: 981
- Based on real Intel microprocessor designs, scaled to 45nm
- No blockage
- Local Skew Distance 600um
- Local Skew Limit 7.5ps



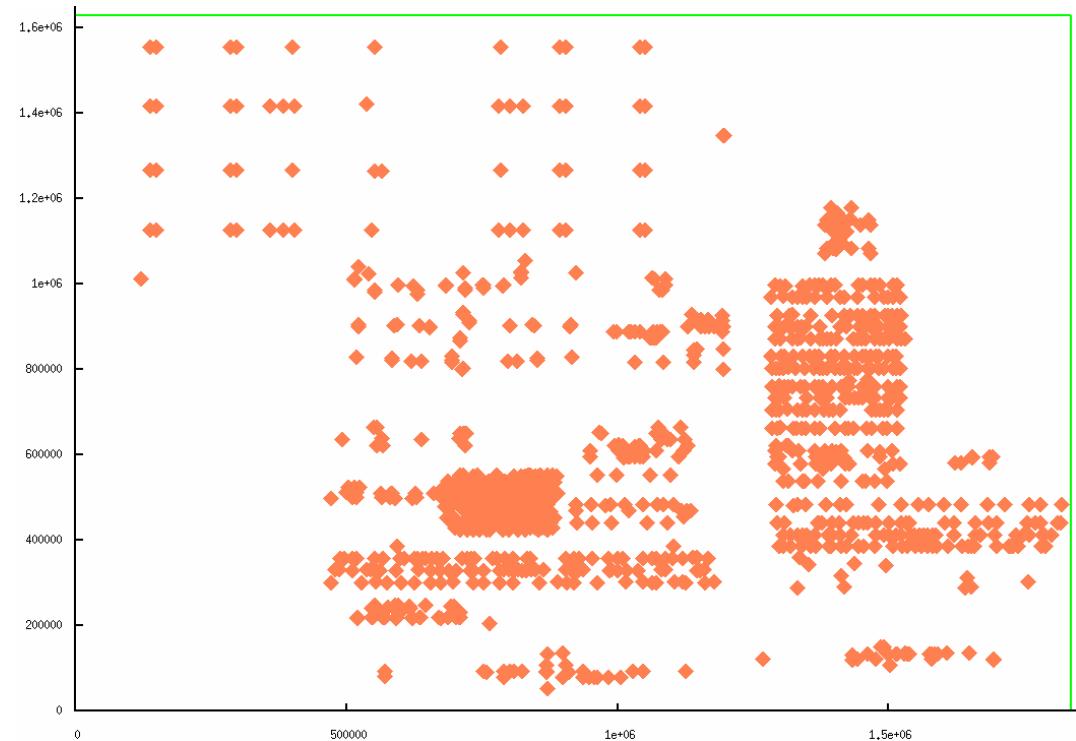
ispd10cns07

- Area: 3.7mm²
- # sinks: 1915
- Based on real Intel microprocessor designs, scaled to 45nm
- No blockage
- Local Skew Distance 600um
- Local Skew Limit 7.5ps



ispd10cns08

- Area: 3.7mm²
- # sinks: 1134
- Based on real Intel microprocessor designs, scaled to 45nm
- No blockage
- Local Skew Distance 600um
- Local Skew Limit 7.5ps



Benchmark Summary

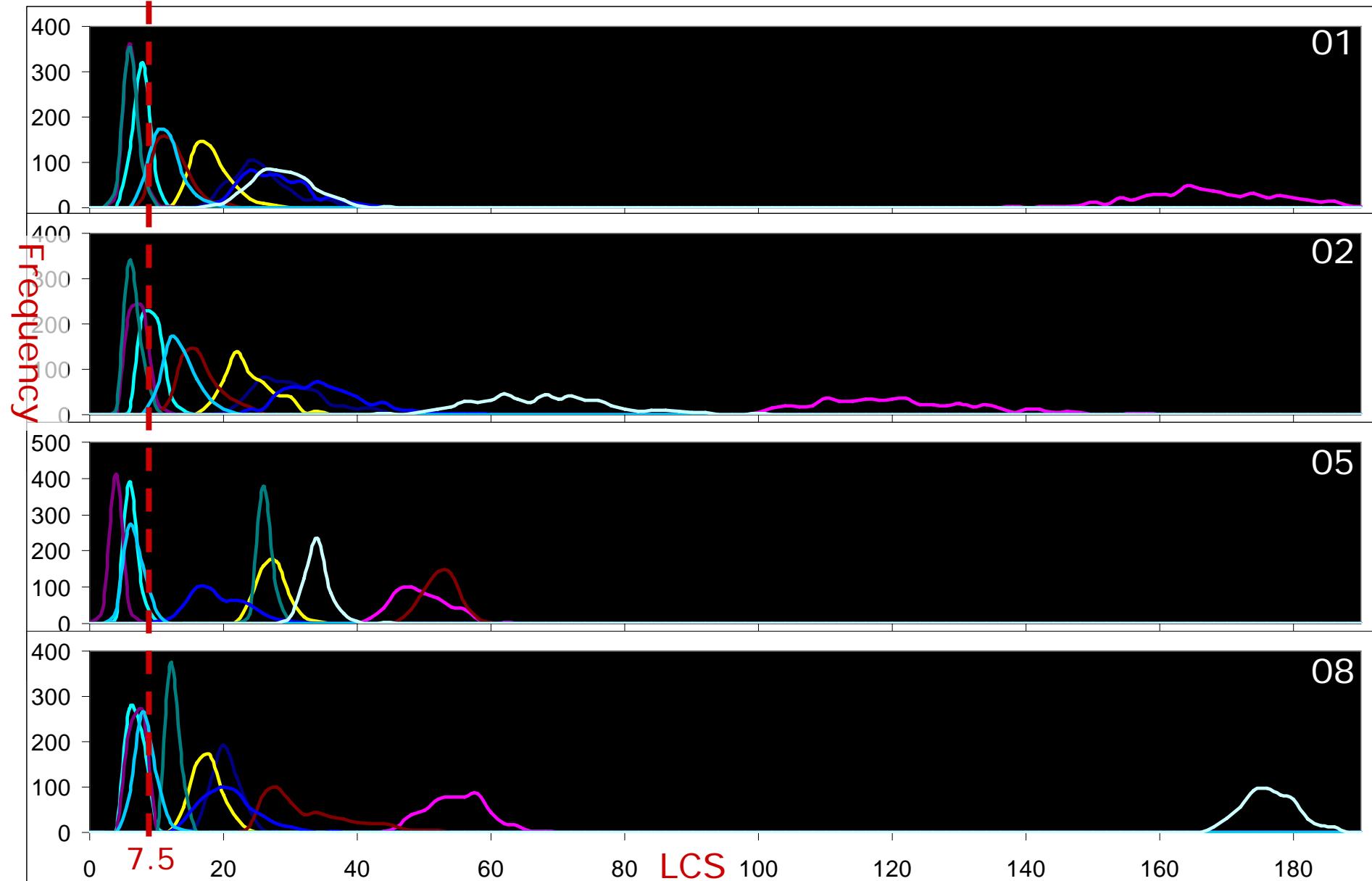
- Only 8 benchmarks are used due to time limit
- More benchmarks will released in the website

Name	# sinks	LCS distance	LCS	width	height	# blockages
ispd10cns01	1107	600000	7.5	8000000	8000000	4
ispd10cns02	2249	600000	7.5	13000000	7000000	1
ispd10cns03	1200	370000	4.9	3071928	492989	2
ispd10cns04	1845	600000	7.5	2130492	2689554	2
ispd10cns05	1016	600000	7.5	2318787	2545448	1
ispd10cns06	981	600000	7.5	1949600	890880	0
ispd10cns07	1915	600000	7.5	2536640	1447680	0
ispd10cns08	1134	600000	7.5	1837440	1628160	0

Evaluation with ngspice Simulations

- Simulation time varies between minutes and 13 hours
 - On a typical Linux machine
(e.g. Intel Xeon X7350 2.93GHz or AMD Dual-Core Opteron 8220@2.8G)
 - Average ~2 CPU-hour per simulations
 - Average simulation results file size 2GB
- 500 simulations per team per benchmarks
 - $500 \times (10 \text{ teams}) \times (8 \text{ test}) \times 2 = 80,000 \text{ CPU-hours}$
- Thanks for IBM Linux Resource
 - 80 simulations at a time
 - 40+ days to finish all simulations
- 2 stage ranking
 - 4 benchmarks to prune out obvious inferior teams
 - Rank only the short-listed teams for all 8 benchmarks

First batch of Results



First Stage Ranking

- 6 teams are pruned
- Median of wLCS **never** meet target for 4 benchmarks

01

		wLCS					
	cpu	mean	min	1st Q	med	3rd Q	max
01	20	24.8	15.4	21.5	24.2	26.9	42.6
06	6	166.8	130.6	159.5	166.2	174.6	198.6
07	6753	17.2	11.8	15.1	16.7	18.8	32.5
08	15	6.7	3.9	6.0	6.6	7.3	11.1
09	1	5.3	3.5	4.5	5.0	5.8	10.7
10	59	11.4	5.8	9.5	10.9	12.9	27.0
15	12015	5.2	3.2	4.4	5.1	5.8	10.1
16	4277	27.0	15.9	23.0	26.4	30.2	46.4
20	3453	10.5	6.0	8.8	10.2	11.7	18.7
22	1191	27.9	16.8	24.7	27.7	30.9	46.3
01	80	29.1	19.0	24.9	28.5	32.3	50.5
06	6	120.1	94.2	110.9	118.7	128.6	163.0
07	14711	22.9	15.0	20.3	22.3	25.1	36.6
08	176	8.3	4.8	7.2	8.1	9.1	14.4
09	0	6.3	4.1	5.5	6.1	6.8	10.8
10	158	15.6	9.4	13.3	15.0	17.3	29.8
15	25969	5.6	3.5	4.8	5.5	6.1	9.2
16	11688	34.5	22.1	29.8	33.6	38.0	66.9
20	10178	12.5	7.6	10.8	12.2	14.0	23.5
22	113184	66.8	43.5	59.7	66.6	73.1	98.8

02



05

		wLCS					
	cpu	mean	min	1st Q	med	3rd Q	max
01							FAILED
06	2	48.5	40.2	45.6	48.1	51.3	60.7
07	1380	26.3	20.6	24.7	26.2	27.6	33.1
08	11	5.3	3.5	4.6	5.2	5.8	9.8
09	7	2.9	1.5	2.3	2.7	3.2	6.5
10	70	51.5	44.7	49.8	51.6	53.2	59.0
15	1310	36.8	34.1	36.2	36.8	37.5	39.7
16	5162	18.2	8.8	15.1	17.5	21.2	31.6
20	1367	5.8	2.3	4.8	5.6	6.6	10.4
22	1333	33.0	28.0	31.8	32.8	33.9	42.7
01	8	19.4	13.4	18.0	19.2	20.6	28.8
06	6	53.8	43.1	50.9	53.8	56.8	66.9
07	2466	16.5	10.7	14.9	16.5	17.9	22.9
08	7	5.9	3.8	5.2	5.9	6.6	9.1
09	19	6.2	4.8	5.7	6.1	6.5	9.2
10	27	31.7	22.3	26.7	29.5	35.4	56.5
15	682	11.5	9.7	11.1	11.5	12.0	13.7
16	5323	19.7	11.2	16.8	19.5	22.1	35.1
20	1376	7.5	4.1	6.3	7.3	8.3	15.4
22	43	175.3	164.4	172.6	175.3	178.1	186.3

08

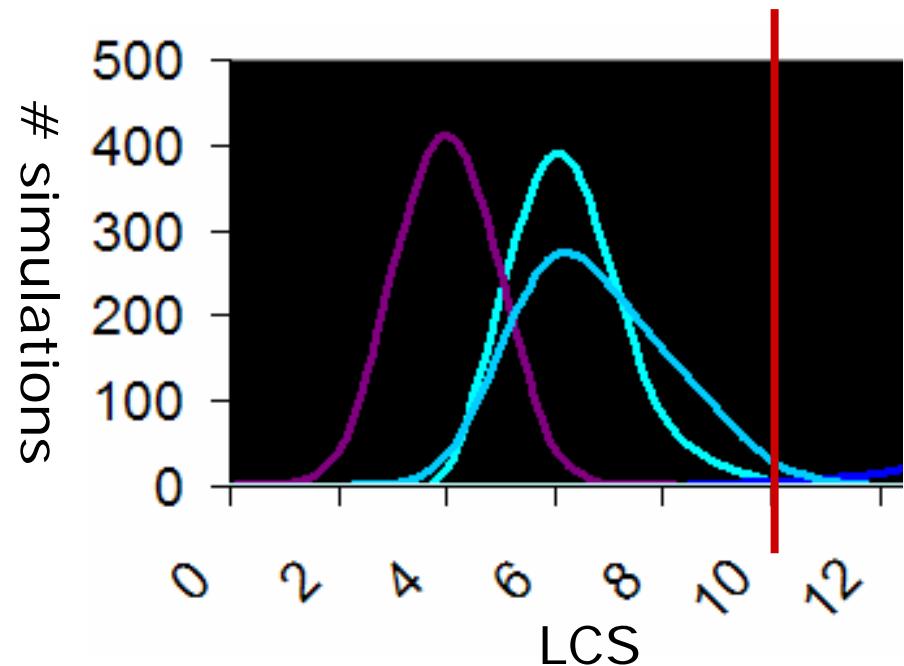


Final top-4 teams

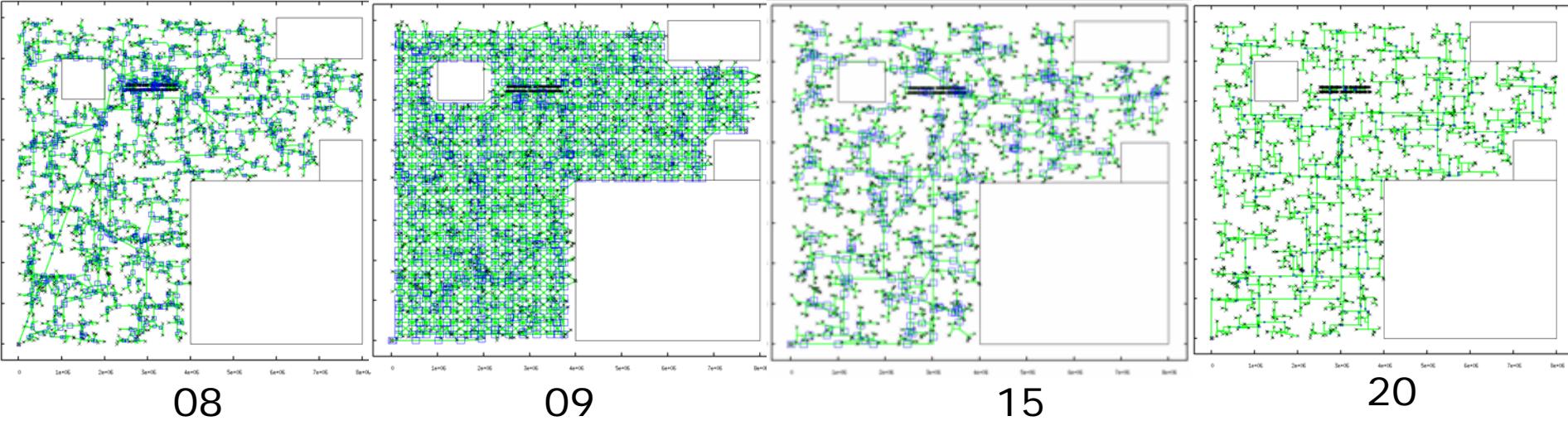
- 08 (NTUclock)
 - National Taiwan University
 - Xin-Wei Shih, Hsu-Chieh Lee, Kuan-Hsien Ho
 - Prof. Yao-Wen Chang
 - 09 (CNSrouter)
 - Chinese University of Hong Kong
 - Linfu Xiao, Zaichen Qian, Zigang Xiao, Yan Jiang
 - Prof. Evangeline F.Y. Young
 - 15 (Contango)
 - University of Michigan
 - Dongjin Lee, Myungchul Kim
 - Prof. Igor L. Markov
 - 20 (Purdue)
 - Purdue University
 - Tarun Mittal, Shashank Bujimalla
 - Prof. Cheng-Kok Koh
- Fully Balanced Clock Tree
 - On Obstacle Avoiding Spanning Graph
 - No SPICE during execution
 - Clock Grid Construction based on local clock distance
 - Connect sinks to nearest grid
 - No SPICE during execution
 - Skew Bounded Clock Tree
 - run SPICE with iterations
 - Post-processing power reduction
 - DME-style tree construction
 - Pre-modeling of inverters
 - run SPICE during execution

Fair comparison of worst local clock skew

- 500 simulations
- Should we compare the worst of 500 simulations?
 - How close is it from the “real worst”
- Ignore the tail
- 95 percentile (~2 sigma)



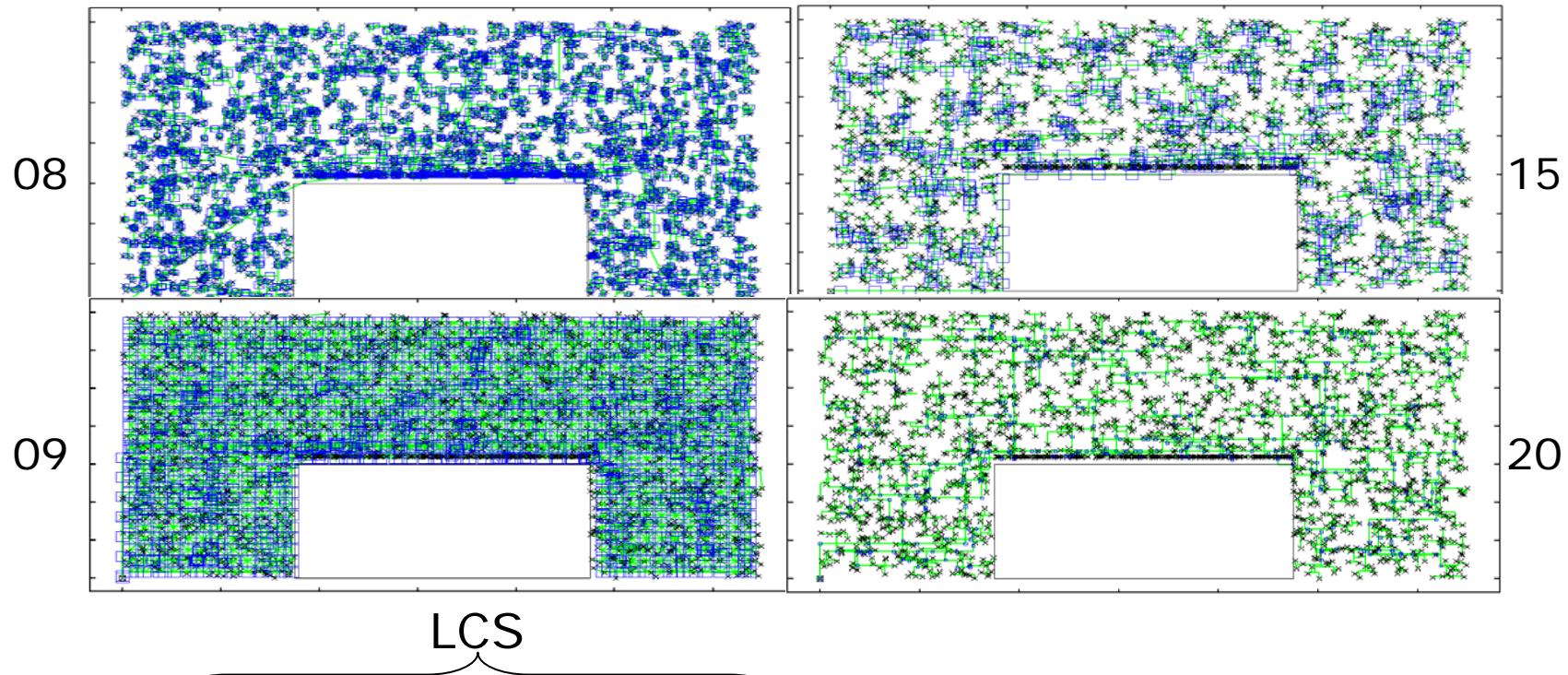
Results for ispd10cns01



LCS

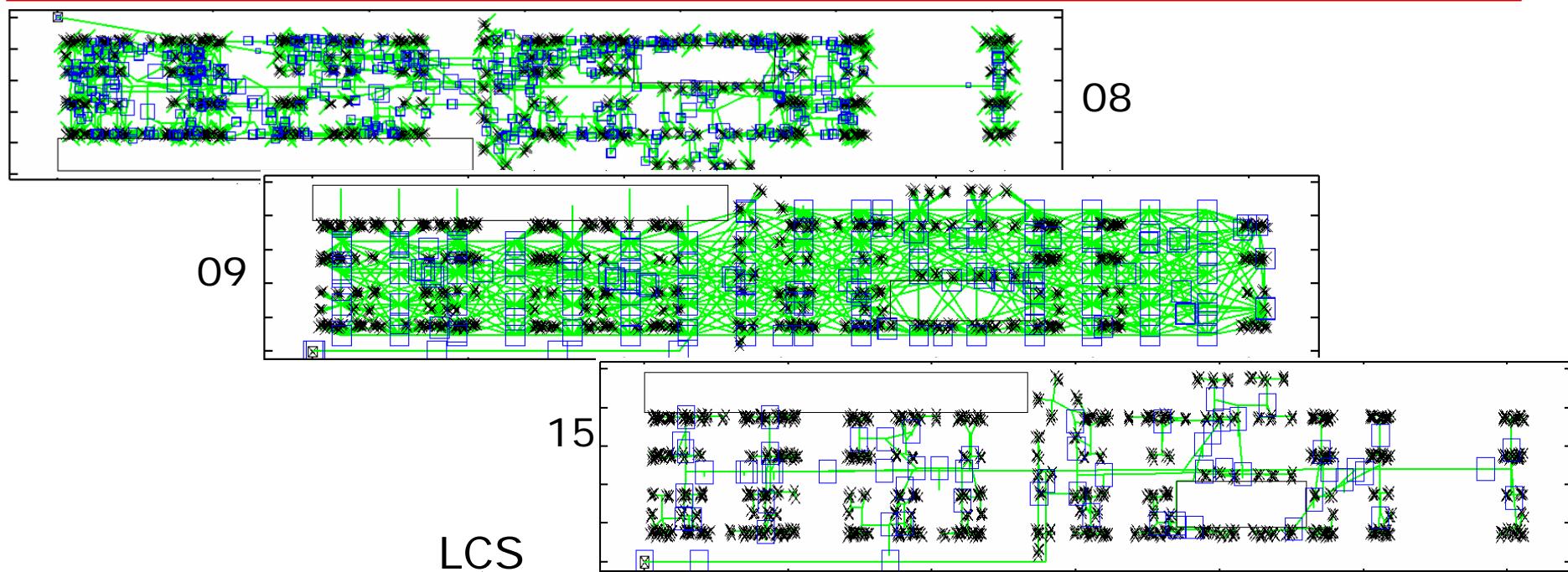
	cpu/s	mean	min	med	95th	max	cap	nom	sink-c	inv-c	wire-c	rank
08	15	6.71	3.87	6.64	8.66	11.14	293887	1.48	18922	159434	115532	3
09	20	5.27	3.51	5.02	7.32	10.74	841207	4.24	18922	489095	333190	2
15	12015	5.16	3.19	5.05	7.01	10.11	198337	1.00	18922	117782	61633	1
20	3453	10.48	5.98	10.20	14.83	18.69	268225	1.35	18922	190325	58978	3

Results for ispd10cns02



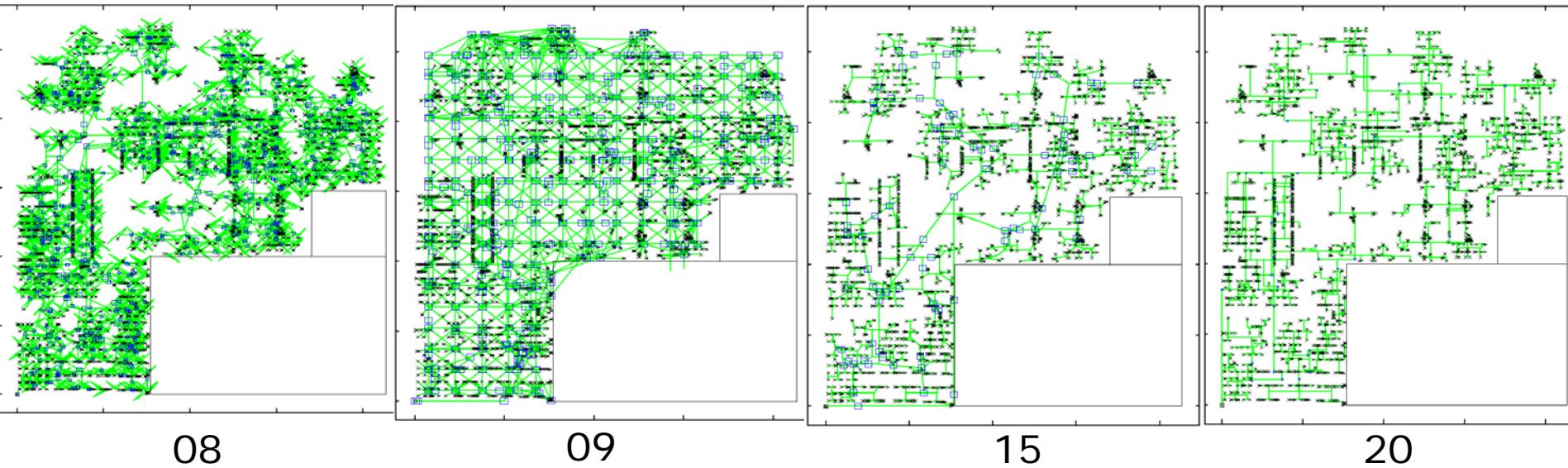
	cpu/s	mean	min	med	95th	max	cap	nom	sink-c	inv-c	wire-c	rank
08	176	8.27	4.85	8.10	10.73	14.44	832483	2.21	39220	558234	235029	2
09	81	6.27	4.13	6.10	8.33	10.83	1E+06	3.87	39220	819375	594334	2
15	25006	5.58	3.45	5.49	7.34	9.24	375863	1.00	39220	227869	108775	1
20	10178	12.51	7.57	12.18	17.03	23.53	506388	1.35	39220	358800	108368	2

Results for ispd10cns03



	cpu/s	mean	min	med	95th	max	cap	nom	sink-c	inv-c	wire-c	rank
08	6	6.82	4.60	6.76	8.63	10.27	167062	2.99	18148	104629	44284	3
09	8	2.07	1.43	2.01	2.70	3.55	162570	2.91	18148	81995	62427	2
15	3840	3.03	1.60	2.95	4.18	5.04	55861	1.00	18148	31097	6615	1
20	FAIL											3

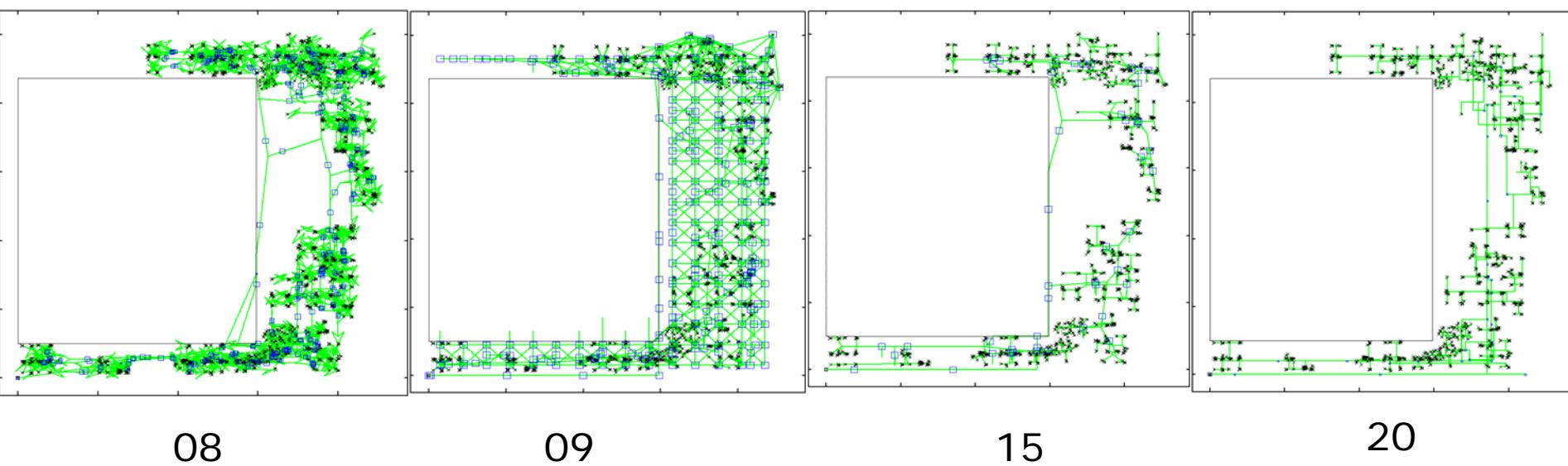
Results for ispd10cns04



LCS

	cpu/s	mean	min	med	95th	max	cap	nom	sink-c	inv-c	wire-c	rank
08	58	7.45	4.85	7.36	9.55	11.36	325206	4.58	12346	181649	131211	3
09	32	2.83	1.65	2.71	3.98	5.74	277151	3.90	12346	177215	87590	2
15	6075	3.26	2.04	3.16	4.46	6.06	71843	1.01	12346	40326	19170	1
20	3051	7.75	4.60	7.51	10.53	13.04	71035	1.00	12346	39790	18899	3

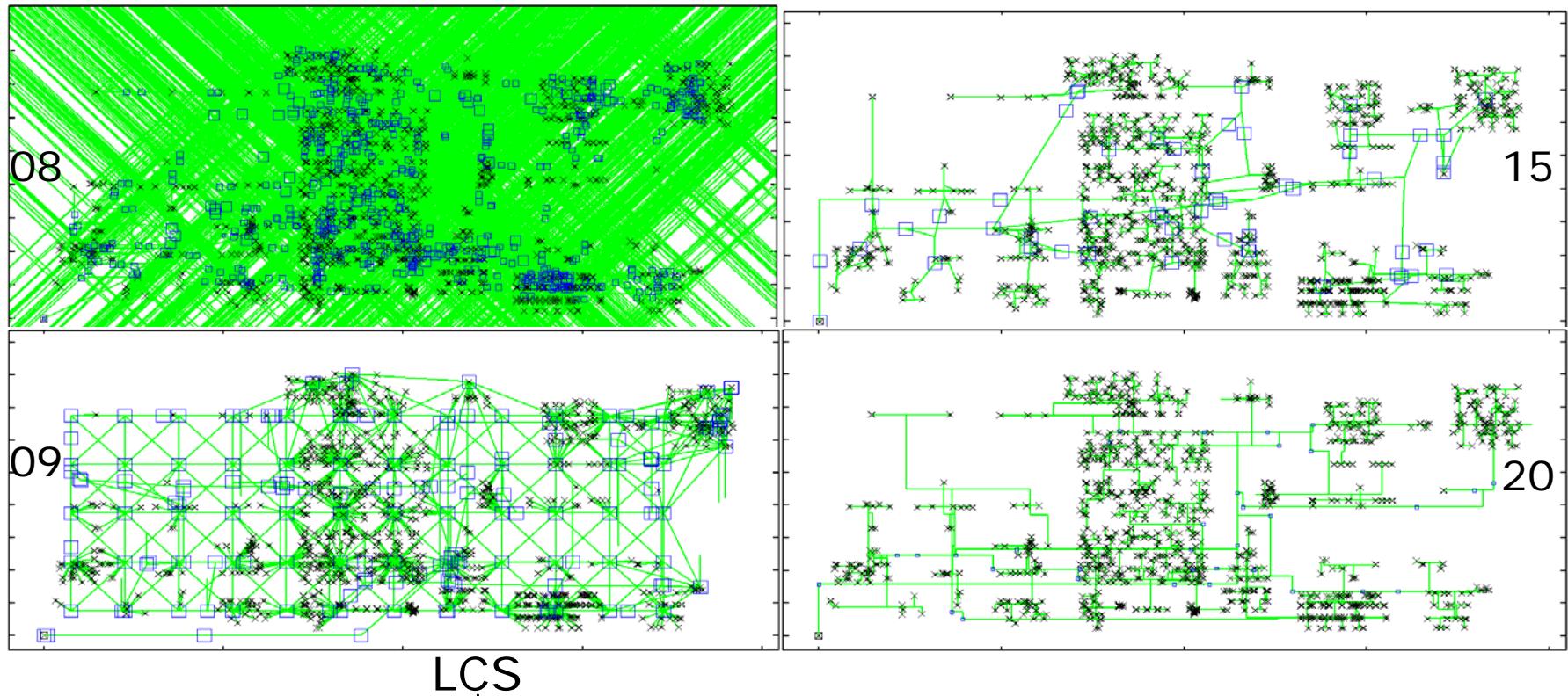
Results for ispd10cns05



LCS

	cpu/s	mean	min	med	95th	max	cap	nom	sink-c	inv-c	wire-c	rank
08	11	5.30	3.49	5.17	6.98	9.79	130389	3.67	5227	65156	60006	1
09	7	2.88	1.51	2.74	4.38	6.51	175580	4.95	5227	120635	49719	2
15	1383	25.19	23.27	25.02	26.91	28.58	35496	1.00	5227	19891	10378	3
20	1367	5.76	2.29	5.62	8.24	10.44	37865	1.07	5227	23230	9409	3

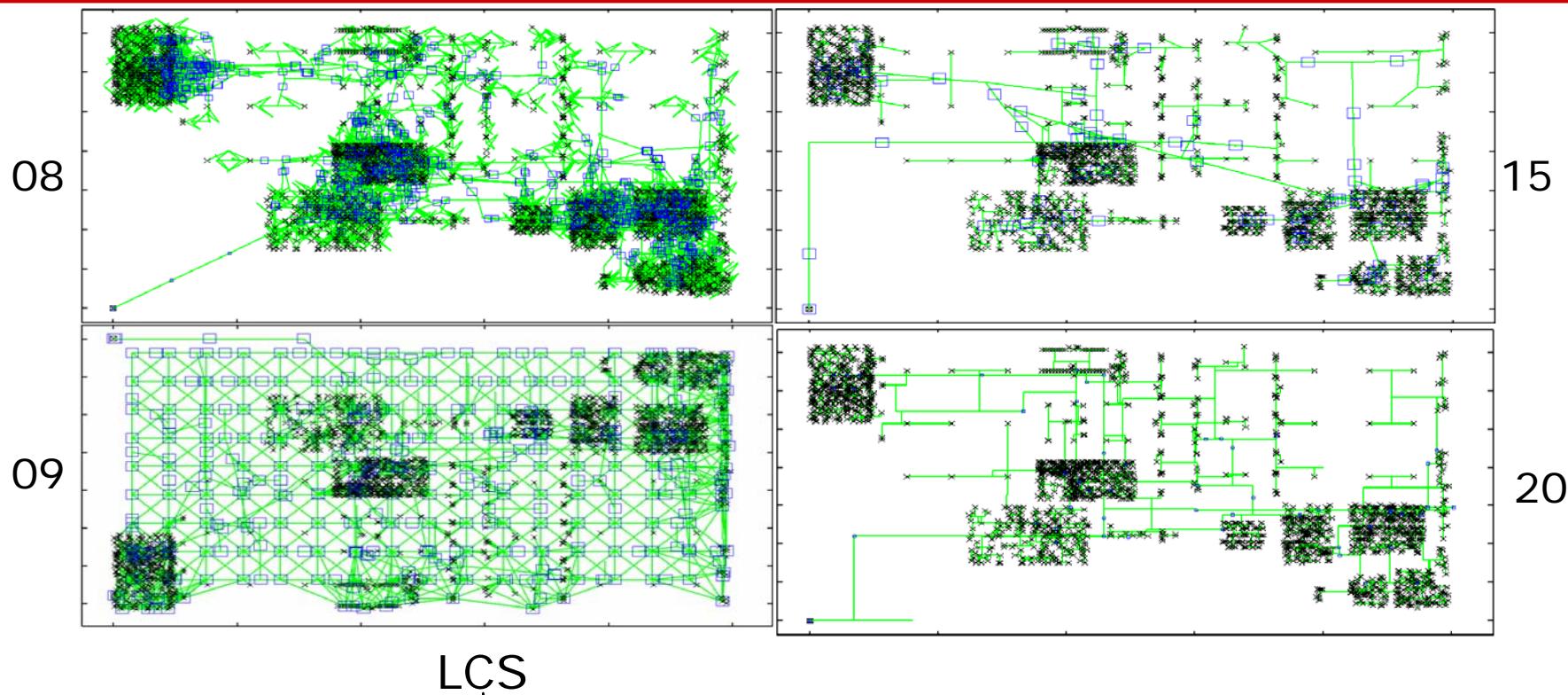
Results for ispd10cns06



LCS

	cpu/s	mean	min	med	95th	max	cap	nom	sink-c	inv-c	wire-c	rank
08	10	406.90	394.09	408.72	416.62	421.29	2E+06	34.50	12576	98619	1465951	1
09	11	12.38	10.17	12.29	14.03	15.12	133312	2.92	12576	83375	37361	1
15	545	23.93	22.30	23.93	24.63	25.22	45719	1.00	12576	25824	7319	1
20	1258	7.36	3.43	7.17	10.45	13.98	46480	1.02	12576	26105	7799	1

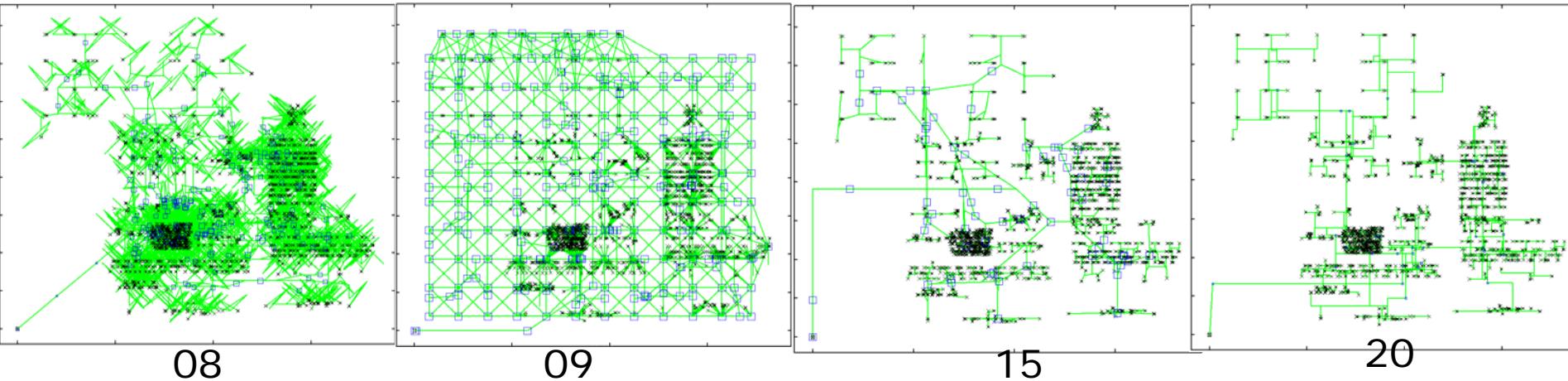
Results for ispd10cns07



LCS

	cpu/s	mean	min	med	95th	max	cap	nom	sink-c	inv-c	wire-c	rank
08	66	6.17	4.30	6.07	8.12	11.29	275597	3.87	18099	130046	127453	2
09	45	12.39	8.35	12.20	15.74	19.65	309242	4.34	18099	201135	90009	2
15	2351	3.41	2.02	3.33	4.58	5.61	72664	1.02	18099	40326	14239	1
20	3319	9.17	5.63	9.03	11.94	14.24	71252	1.00	18099	39100	14053	2

Results for ispd10cns08



LCS

	cpu/s	mean	min	med	95th	max	cap	nom	sink-c	inv-c	wire-c	rank
08	7	5.94	3.76	5.85	7.64	9.05	165883	3.52	13044	42484	110355	2
09	19	6.15	4.85	6.06	7.33	9.21	222786	4.73	13044	147315	62427	1
15	682	11.54	9.67	11.51	12.71	13.66	51515	1.09	13044	29779	8692	2
20	1376	7.46	4.13	7.27	10.17	15.37	47115	1.00	13044	25300	8771	2

Final Results

- First Place
 - University of Michigan (Contango)
- Second Place
 - Chinese University of Hong Kong (CNSrouter)
- Third Place
 - National Taiwan University (NTUclock)

	cpu/s	mean	min	med	95th	max	cap	sink-c	inv-c	wire-c	rank	good
08	44	56.70	52.97	56.83	59.62	62.33	470957	17198	167531	286228	2.125	1
09	15	6.28	4.45	6.14	7.97	10.17	446847	17198	265018	164632	1.750	5
15	6487	10.14	8.44	10.06	11.48	12.94	113412	17198	66612	29603	1.375	5
20	3000	7.56	4.20	7.37	10.40	13.66	131045	14929	87831	28285	2.375	0

LCS

Averages

Conclusion

- Thanks to all hard-working students
 - It is a workshop rather than a contest
- Benchmarks derived from microprocessor designs
 - None of the team produce acceptable solutions for all benchmarks
 - Going to see more papers upon these benchmarks
- Clock network synthesis is very hard in real world
 - Designer's prospectives
 - EDA's prospectives
- For sub-5ps skew with variations
 - Tree or Grid?