Power Grid Analysis Challenges for Large Microprocessor Designs

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Introduction

• Chip size and complexity has grown exponentially over the years
• Power distribution network (or power grid) is an extremely important component of processor design
• Power grid design and analysis is a very challenging task because of:
  – increasing complexity and operating frequency
  – shrinking feature size
  – sensitivity to supply voltage variations
  – low power demand
• Special purpose efficient high capacity tools set is required
Oracle Sparc Design: Data Size and Trend

Largest Block Size

<table>
<thead>
<tr>
<th>Process technology node</th>
<th>Total number of devices x 1B</th>
</tr>
</thead>
<tbody>
<tr>
<td>40nm</td>
<td>0</td>
</tr>
<tr>
<td>28nm</td>
<td>0.5</td>
</tr>
<tr>
<td>20nm</td>
<td>1</td>
</tr>
<tr>
<td>14nm</td>
<td>2.5 (Projected)</td>
</tr>
</tbody>
</table>
Typical Power Grid Design
Power Grid Extraction Challenges

- Extraction is a critical part of design analysis sign-off methodology
- Meantime, it can be an extremely complex task due to the processor design size
- Severe run time and capacity issues has been identified when running EDA vendor extraction tools for large design with >1B resistors
- 14nm design will grow 2-3X in size
- High capacity demand needs to be addressed by extraction methodology and tools
Power Grid Extraction Challenges

Extraction Memory Usage Profile

- LVS cross-reference data generation
- Netlist generation (10.5 Hrs)

Memory Usage, GB vs. Run Time, Hours
Why Early Power Grid Analysis?

- Too many design iterations at signoff
- Full extraction runs into the performance and capacity issues
- Transistor level simulation for tap currents analysis is accurate but slow
- Methodology to refine power grid at various design stages [R.Panda, et.al., DAC-98]
- IR drop estimation at composition stage:
  - fast 1D extraction
  - gate level static analysis for tap currents
  - R-only power grid analysis
Early Power Grid Analysis

Fast/Low Accuracy

1. High Level Description
2. Synthesis
3. Power Grid Planning
4. 1D Extraction
5. Composition
6. Final Extraction
7. Sign Off

Slow/High Accuracy

Power Grid Estimation

Gate Level Static Analysis

Early Power Grid Analysis

Transistor Level Simulation

Power Grid Simulation
Bulk Grid Analysis
Bulk Grid Analysis Challenges

- Tap points for transistor currents are not localized: substrate resistance extraction is required

![Diagram showing transistor components and substrate resistance](image)
Bulk Grid Analysis Challenges

- Bidirectional switching large currents charging transistor capacitors must be analyzed along with small unidirectional leakage current.
- Results interpretation is different from the regular power grid.

![Diagram showing Bulk Current, Latchup (short circuit), Leakage current, and Device performance degradation.](attachment:image.png)
Design Style: Flat vs Hierarchical

- Hierarchical design is a natural solution for capacity problem
- However there are techniques made it attractive to compose a flat design down to library cells level:
  - advances in place and route technology
  - opportunities for accurate timing analysis
  - manual optimization
- Highest metal density areas placed within library cells helps to reduce the data size
- However the overall size is still too large
- Artificial hierarchy: introduces too many currents across the block boundaries
Simulation Techniques: Hierarchical

- Global and multiple local power grids
- Hierarchical power grid analysis [M. Zhao, et al., DAC-2000]
- Block size and number of ports are rapidly growing
Simulation Techniques: Solutions

- Multigrid approach [F.Najm, et.al, ICCAD-2001]: fast, but not accurate, difficult to use for irregular structures
- Model Order Reduction [L.He, et.al., DAC-2006]: inefficient for the large number of ports
- Currents locality effect [E.Chiprout, et.al., ICCAD-2004; A.Korobkov, et.al., PIERS-2009]: better run time/accuracy tradeoff, but scalability is limited
- Iterative methods like Random walks [S.Nassif, et.al, DAC-2003], Successive over-relaxation [M.Wong, et.al., ICCAD-2005]: memory efficient and easy to parallelize but slow
# Simulation Techniques: Solutions

<table>
<thead>
<tr>
<th>Direct Methods</th>
<th>Iterative Methods</th>
</tr>
</thead>
<tbody>
<tr>
<td>Fast but memory inefficient and difficult to parallelize</td>
<td>Slow but memory efficient and easy to parallelize</td>
</tr>
<tr>
<td>Dynamic vector based analysis for smaller design</td>
<td>Static or pseudo-dynamic analysis for larger design</td>
</tr>
<tr>
<td>Memory usage can be addressed by efficient parallel distributed analysis with multiple processes</td>
<td>Performance can be addressed by the improved initial guess and parallel runs with multiple threads</td>
</tr>
</tbody>
</table>

- Transient analysis is problematic, however direct solver in combination with constant time step provide some improvement
- Combined direct and iterative methods does not provide much performance gain while use more memory and reduce opportunities for parallel execution
Simulation Techniques: Direct Solver

- Direct solver is fast, but how to reduce memory?
- Solution: distributed parallel linear solver
- Extensively used outside EDA (structural mechanics, fluid dynamics, etc.)
Distributed Linear Solver: Run Time

Block level power grid with 86M nodes, 356M devices

- 1 process
- 2 processes
- 4 processes

Expect similar scaling for larger blocks
Distributed Linear Solver: Memory

Block level power grid with 86M nodes, 356M devices

Expect similar scaling for larger blocks
Design Debugging Aid

- Layout editor capacity challenge
- Graphic interface overlay EM violations to layout
- Tracer between IR violation and source
- Automated fixer tools
Future Challenges (14nm and Beyond)

- Growing design size and the number of devices will drive the power grid size
- More EM and IR issues due to:
  - higher frequency
  - reduced supply voltage
  - dynamically switching gated grids
  - narrower, thinner and longer wires
- Inductance will play more important role in extraction and analysis, along with package model
- More complex parasitics for 3D devices (FinFET), multiple new sources of variability
- FinFETs will dramatically increase power density: reliability and thermal analysis are required
Conclusions

- Power grid size for processor design is rapidly growing but EDA vendors are late to respond
- Parasitics extraction complexity is a challenge, tools and methodologies must comply
- Bulk grid analysis is an important part of the power grid analysis supported by the same tools set
- Hierarchical power grid design can help with both extraction and analysis but does not solve all issues
- There are multiple simulation strategies, but no perfect solution available
- Parallel and distributed execution is a must
- Many new challenges come up with 14nm process, need to be addressed as soon as possible
Q & A